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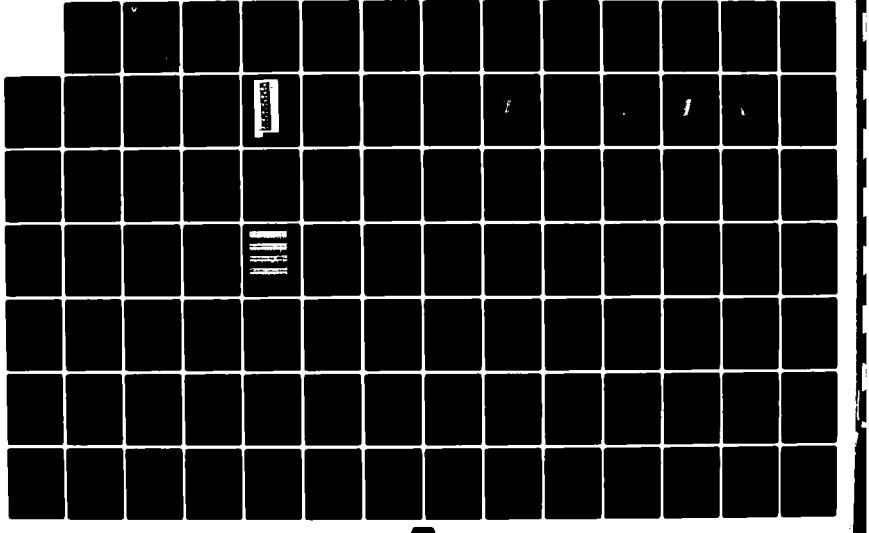

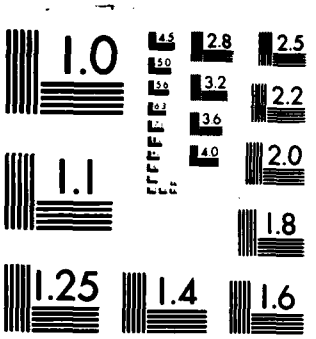

RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CECOM-82-C-J231

500-WATT SOLID-STATE RF POWER AMPLIFIER AM-7209( )/VRC

M. Balasis, W. Boller, W. Coleman, M. Harris
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18 MARCH 1983

SECOND QUARTERLY REPORT FOR PERIOD 15 DECEMBER 1982 - 15 MARCH 1983

Prepared For:

CECOM

US ARMY COMMUNICATIONS - ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Progress in amplifier module circuit design and development is documented in this second quarterly report.

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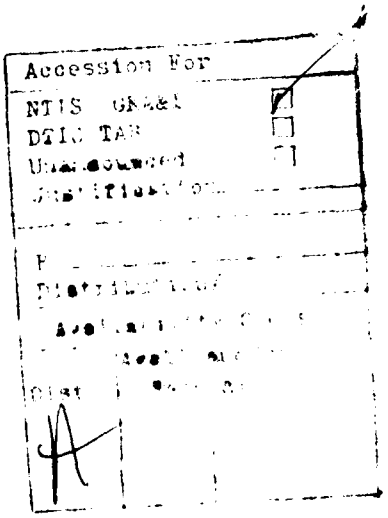

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1.0 INTRODUCTION

The development, fabrication, and test of three advanced development model 500-watt VHF power amplifiers to be used to increase the output of presently-deployed RT-524 (VRC-12) VHF radios and future equipment such as the frequency hopping SINCGARS-V equipment is documented in this report. The power amplifier, as defined in US Army Communications-Electronics Command contract DAAB07-82-C-J231, is a state-of-the-art stand-alone design utilizing a combination of the latest design techniques in RF elements, control circuits, packaging techniques, and amplifier architecture.

The circuit designs and breadboard test results of the development effort to date are presented in this second quarterly technical report, which is written in response to contract line item number 0004, data item sequence number C001 of the referenced contract. Also included in this report are a description of the current design status and a listing of expected effort for the next reporting period.

2.0 AMPLIFIER DESIGN

The major effort of the past quarter has concentrated on designing, breadboarding, and testing circuits to perform the amplifier functions as described in the previous status report. The first quarterly report has been used as a guide in partitioning the module functions and in defining the amplifier interfaces. In parallel with the design efforts, module packaging has been continuing in both the case and housing areas and in the layout of the amplifier modules. In many instances, the electrical designs of modules or component selections have been changed to simplify the packaging effort or to allow the function to be achieved within the space bounds established.

The design effort accomplished during the first two calendar quarters on the power amplifier development project is described in detail in the remainder of Section 2 of this report. Each amplifier module design is separately discussed, along with a presentation of the results of integrating the overall RF amplifier chain. Detailed block diagrams and schematics of the circuit designs and the supporting design analyses are presented for the major circuit elements. Results of tests performed are also presented in this report. Continued testing and layout tasks are currently in progress, and these efforts are resulting in further refinement of the design as the final packaging efforts are completed. Therefore, some minor changes are anticipated in the fine details of the data presented. The report documents the current design status.

This quarterly report is organized in a similar manner to the previous report, with the overall amplifier design description followed by the individual amplifier internal module descriptions in order of the assigned reference designations. At the conclusion of the electrical and mechanical design descriptions, a summary of the current status and a description of the anticipated effort for the next quarter are listed.

2.1 VHF POWER AMPLIFIER

The VHF power amplifier is a rugged, reliable, efficient, high performance unit capable of fully automatic operation with a variety of VHF driver transmitters. Operator interface with the amplifier is limited to connecting primary power and RF input and output cables, and turning the unit on. The operator controls are limited to an output power selection switch which permits selection of either the full 500-watt nominal output or a reduced 250-watt level, and a display control switch. The available display modes are: output forward power, reflected power, BITE code, and display off. Frequency control and keying interfaces are internally controlled, based on the RF drive signals applied.

The amplifier is composed of 17 major modules. Figure 2.1-1 is a block diagram showing the amplifier functional partitioning. Basically, the input is attenuated, then amplified by a variable gain driver amplifier and six paralleled output amplifiers before being filtered, sampled, and routed to the RF output connector. Support circuits include power supplies, RF power control loops, status measuring and reporting circuits, and the system processor. These circuits keep track of amplifier operation and control the RF output power level.

2.1.1 Electrical Tests

Testing of a breadboard version of the entire RF portion of the power amplifier has verified the performance expectations of the design. The nominal output power level was set to 540 watts, or 0.3 dB above the rated 500-watt output, for all performance data measurements. Table 2.1.1-1 is a list of measured data for input drive levels of 3, 6, and 9 watts with the input RF processor set at 0 dB attenuation. At higher drive levels, attenuators are switched in-line, limiting the RF level applied to the driver amplifier, and improving the input VSWR. The low pass effect of the six-way RF power combiner together with the low harmonic output of the biased push-pull amplifiers results in extremely low harmonic output levels from the 500-watt power amplifier. Table 2.1.1-2 lists the relative harmonic levels present at the combiner output port, the measured attenuation of the appropriate low pass filter, and the resulting theoretical harmonic output from the amplifier. The -67 dBc limit specified in MIL-STD-461A, Notice 4 is exceeded by at least 9 dB, worst case. The photograph of Figure 2.1.1-1 shows the breadboard power amplifier including the six-way RF power splitter, the six-way RF power combiner, and the main heatsink containing the six output amplifiers and their associated temperature compensated bias supplies.

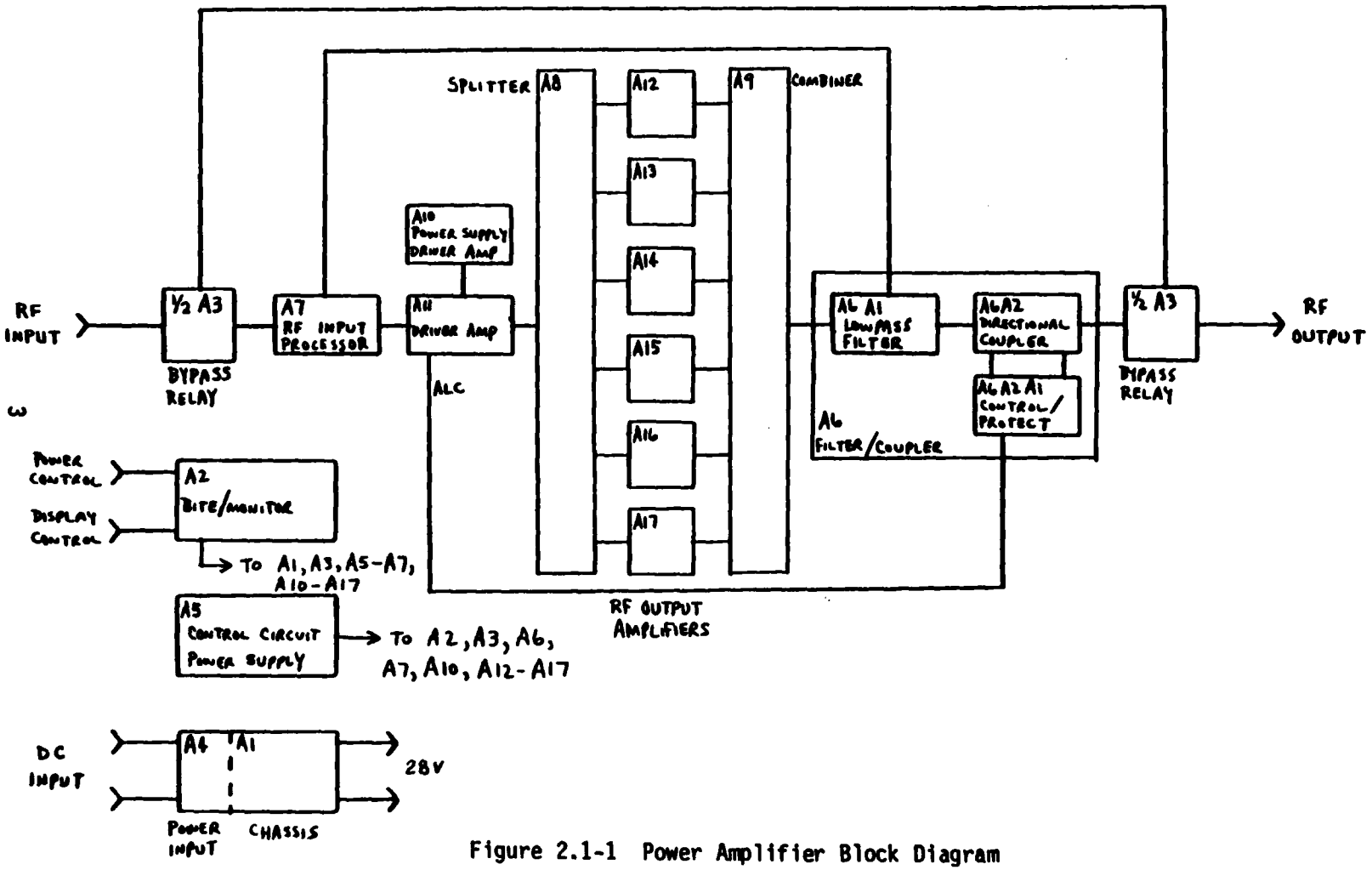


Figure 2.1-1 Power Amplifier Block Diagram

Table 2.1.1-1 Breadboard 500-Watt VHF PA Test Data

PARAMETER		FREQUENCY (MHz) P_{out} = 540 watts						
		30	40	50	60	70	80	88
P_{IN} (W)		3.0	3.0	3.0	3.0	3.0	3.0	3.0
P_{REF} (W)		.22	.17	.11	.00	.00	.05	.00
VSWR		1.74	1.62	1.47	1.0	1.0	1.30	1.0
V_{AGC} (V)		+4.6	+2.5	+3.8	+3.0	+4.1	+4.2	+5.0
I_{DRIVER} (A)		2.2	3.0	4.6	4.3	5.9	6.0	6.2
P_{IN} (W)		6.0	6.0	6.0	6.0	6.0	6.0	6.0
P_{REF} (W)		.41	.24	.11	.00	.00	.00	.00
VSWR		1.71	1.50	1.31	1.0	1.0	1.26	1.0
V_{AGC} (V)		+.60	+.85	+2.1	+2.1	+1.8	+2.0	+2.8
I_{DRIVER} (A)		2.3	2.9	4.0	3.9	5.0	5.0	5.2
P_{IN} (W)		9.0	9.0	9.0	9.0	9.0	9.0	9.0
P_{REF} (W)		.59	.30	.10	.00	.00	.10	.08
VSWR		1.69	1.45	1.24	1.0	1.0	1.24	1.21
V_{AGC} (V)		-.55	-.35	+.70	-.45	+.60	+3.5	+1.15
I_{DRIVER} (A)		2.4	2.8	3.8	3.8	4.6	4.8	5.4
OUTPUT AMPLIFIER CURRENTS	I1	6.3	6.8	6.2	5.9	5.2	8.8	6.4
	I2	6.7	5.3	6.0	6.7	6.0	7.8	7.2
	I3	7.1	5.8	6.8	7.0	7.2	4.8	7.0
	I4	7.0	7.0	6.4	7.2	7.6	5.6	4.7
	I5	6.5	5.9	5.4	7.8	6.6	5.4	6.4
	I6	7.7	6.1	4.4	7.4	7.3	5.8	5.5

Table 2.1.1-2 Power Amplifier Harmonic Output Levels

PARAMETER	HARMONIC	FUNDAMENTAL FREQUENCY (MHz) 30	40	50	60	70	80	88
AMPLIFIER	2	-52	-52	-47	-54	-57	-60	-66
HARMONIC	3	-18	-27	-45	-60	-58	-62	-68
LEVELS	4	-53	-70	-	-	-	-	-
(dBc)	5	-64	-	-	-	-	-	-
FILTER	2	75	53	70	55	60	65	75
REJECTION	3	58	80	90	65	70	75	80
(dB)	4	75	90	-	-	-	-	-
	5	100	-	-	-	-	-	-
RESULTING	2	-127	-105	-117	-109	-117	-125	-141
AMPLIFIER	3	-76	-107	-135	-125	-128	-137	-148
HARMONIC	4	-128	-160	-	-	-	-	-
OUTPUT	5	-164	-	-	-	-	-	-
(dBc)								

Notes:
1. "-" in amplifier harmonic output table indicates a measured level below -70 dBc.
2. "-" in filter rejection table indicates a measured level below -100 dBc.
3. Power output level of harmonic level tests is 500 watts.

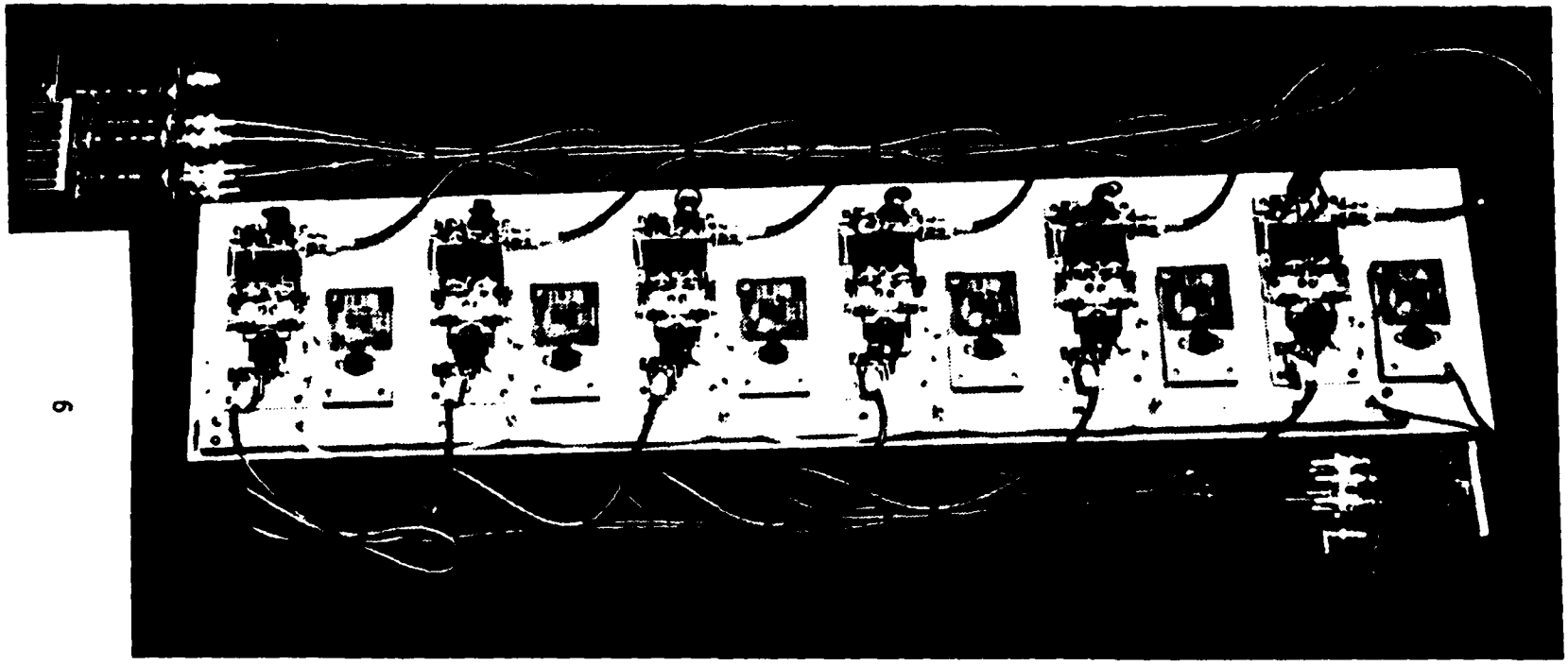


Figure 2.1.1-1 500-Watt VHF Power Amplifier Breadboard

2.1.2 Amplifier Mechanical Design

The mechanical design of the 500-watt amplifier is proceeding as outlined in the original proposal with few changes. The overall design concept remains as proposed with the six plug-in amplifier modules and the single driver module being mounted to the periphery of the main case. Cooling of these modules is accomplished by natural convection and radiation with no forced air required.

2.1.2.1 Thermal Analysis

During the development of the overall packaging design, the thermal dissipations of all the module elements have been continuously monitored and analyzed. No major detrimental changes have occurred since the original proposal. Complete compliance and improvement on the specification requirement of a 50 percent duty cycle with one minute "on" and one minute "off" is predicted.

2.1.2.2 Overall Mechanical Design Concept

During the design and development of the mechanical packaging design some small changes have been made to the original design concept. Figure 2.1.2.2-1 depicts the design as now being produced for the deliverable units. The overall dimensions have slightly changed from 20.50 inches wide, 8.00 high, and 13.25 deep to 21.562 wide, 7.625 high, and 13.375 inches deep. The revised dimensions allow the specification requirement of a total volume of 2200 cubic inches with a maximum depth of 14.00 inches to be achieved.

The interior modules have been rearranged to facilitate the RF flow. A small flex cable has been added between the main module interconnect printed wiring board and the plug-in power amplifier modules. This additional flex cable eliminates a mechanical tolerance buildup problem, facilitating future production.

The original one-piece front panel concept has also been changed to a design with three separate functional panels. Figure 2.1.2.2-2 depicts the present design. The three functional panel assemblies are: the input DC power conditioning panel, the digital display panel, and the RF connector panel. The input DC power conditioning panel contains the input power connector, a reset power circuit breaker, and a power on-off switch. The second panel contains a digital display with a control switch for selecting the forward power, reflected power, or BITE readout. The panel also includes a high/low RF power level switch. All of the control circuitry is located behind this panel. Removing this panel exposes the printed circuit board, permitting complete troubleshooting of the entire amplifier. The RF connector panel contains the RF input and output type "N" connectors. The RF bypass coaxial switch is mounted to the rear of the connector panel.

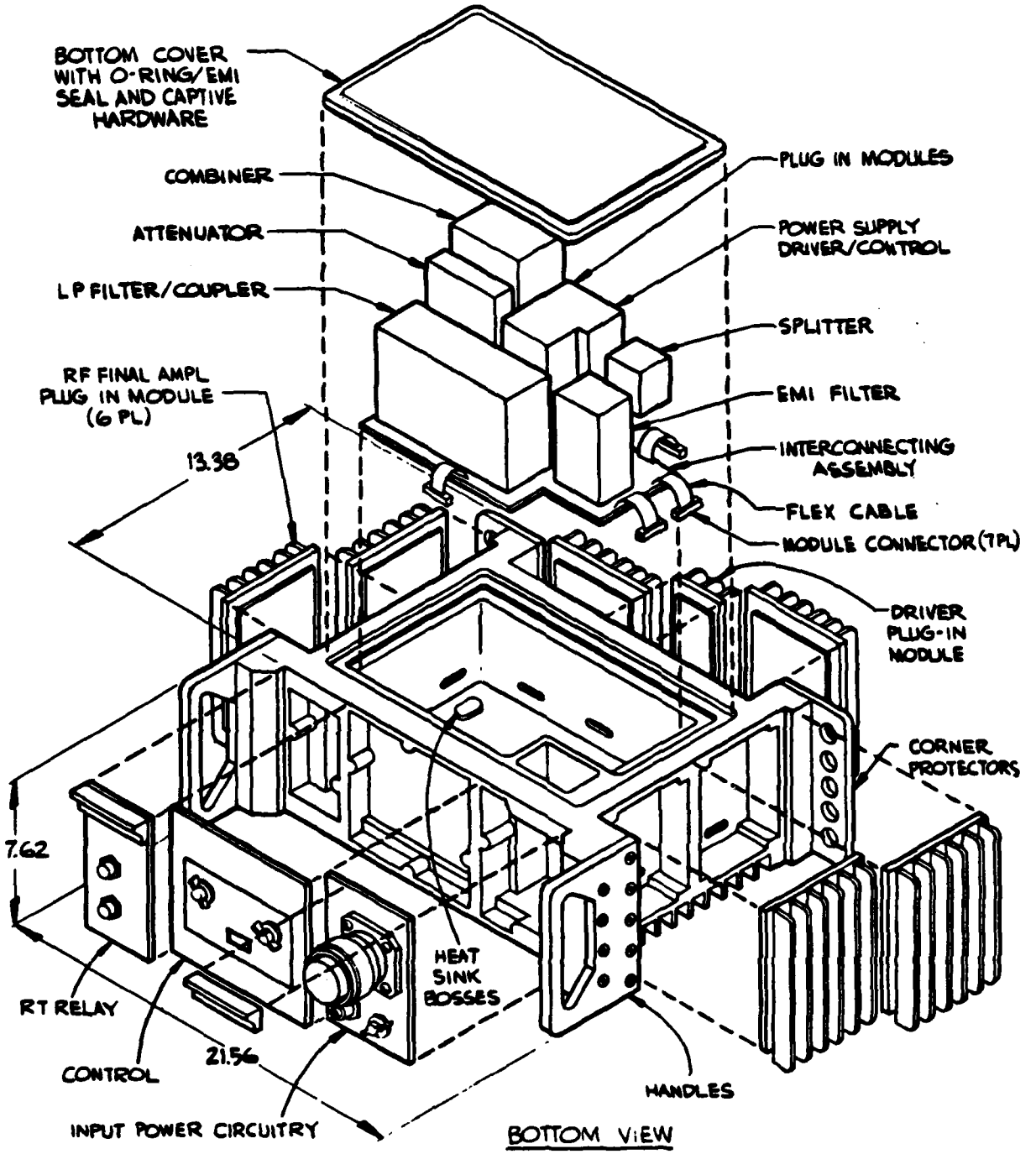


Figure 2.1.2.2-1 Power Amplifier Exploded Bottom View

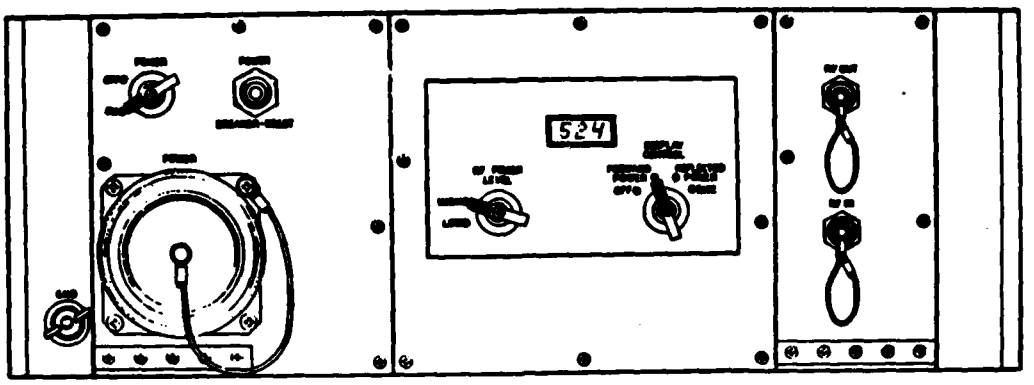


Figure 2.1.2.2-2 Front Panel Layout

2.1.2.3 Stress Analysis

An extensive mechanical stress analysis of the front and rear corners of the main case has been performed to insure compliance with the four-foot drop test as specified by MIL-STD-810 Procedure II, Method 516.2. The stress analysis was performed by Dr. Oline of The University of South Florida, utilizing the "Super Sap" computer finite element analysis program. Results of the analysis show that the case, handles, and mounting hardware are well within their maximum stress levels, with the maximum stresses present in the bolts that mount the handles to the case. Fourteen different load cases were analyzed. For one analyzed condition, Figure 2.1.2.3-1 shows the finite element structural model of the front handle; Figure 2.1.2.3-2 shows the stress contour of the handle; Figure 2.1.2.3-3 shows the deformation amplified 50 times; Figure 2.1.2.3-4 shows the finite element structural model of the rear corner; Figure 2.1.2.3-5 shows the deformation of the corner amplified 100 times. As a result of the analysis, the capability of the case to handle the stress of the drop test has been verified, and higher strength, larger diameter mounting bolts have been included to prevent breakage.

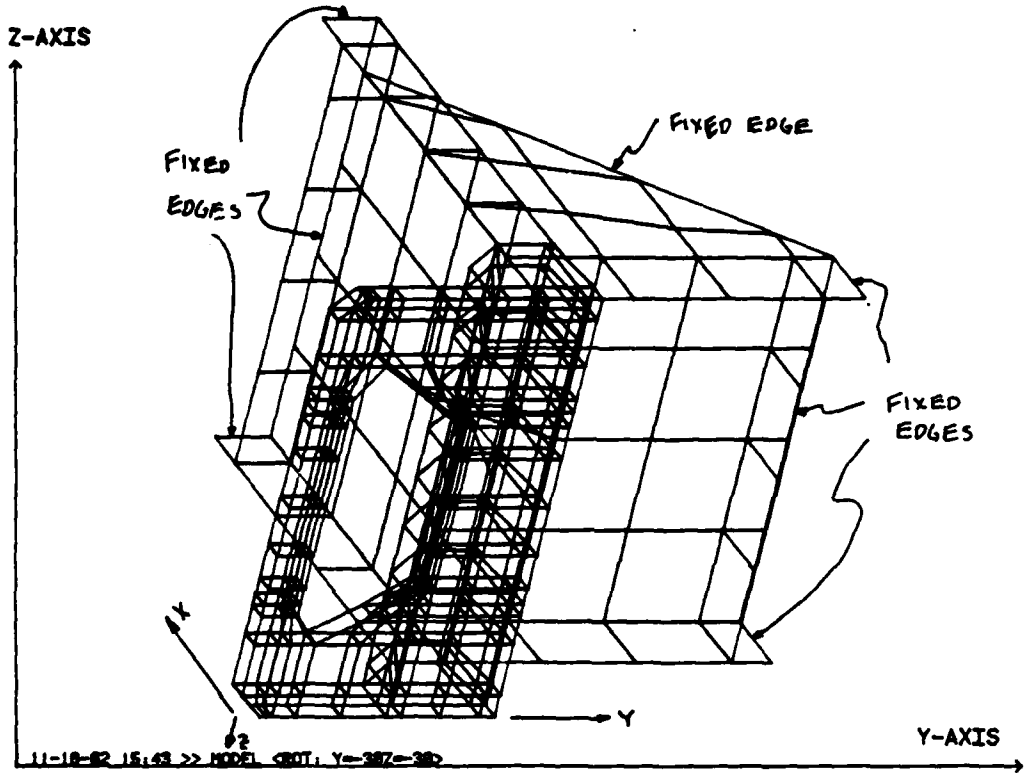


Figure 2.1.2.3-1 Front Handle Finite Element Model

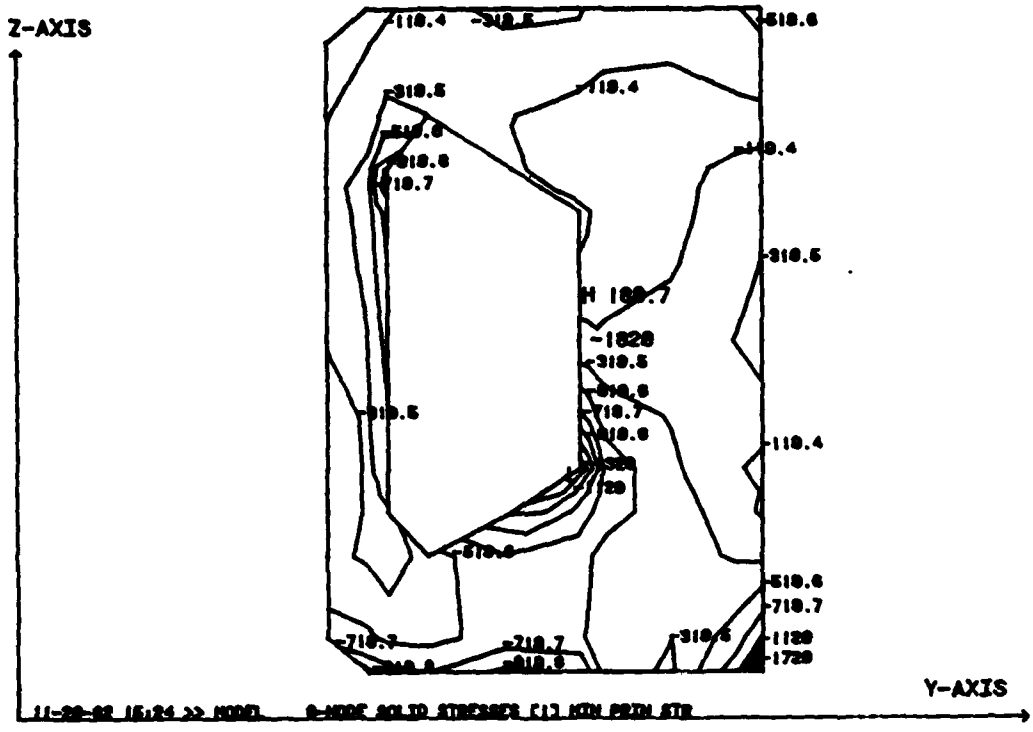


Figure 2.1.2.3-2 Front Handle Stress Contour

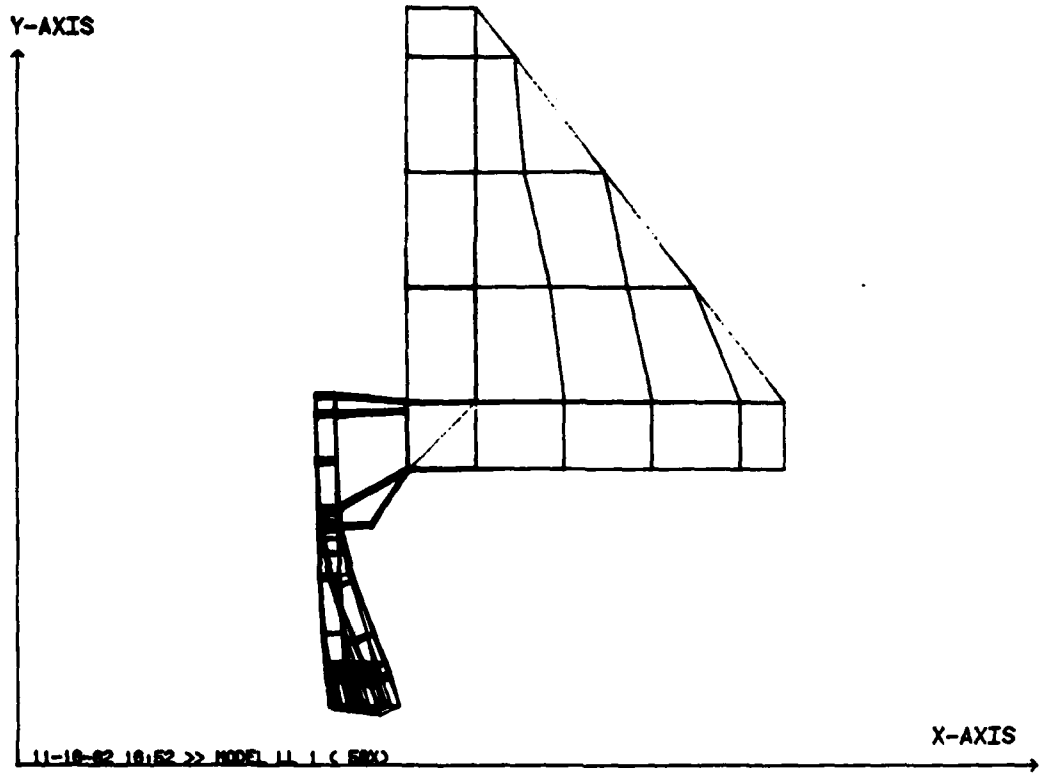


Figure 2.1.2.3-3 Front Handle Deformation (Amplified X50)

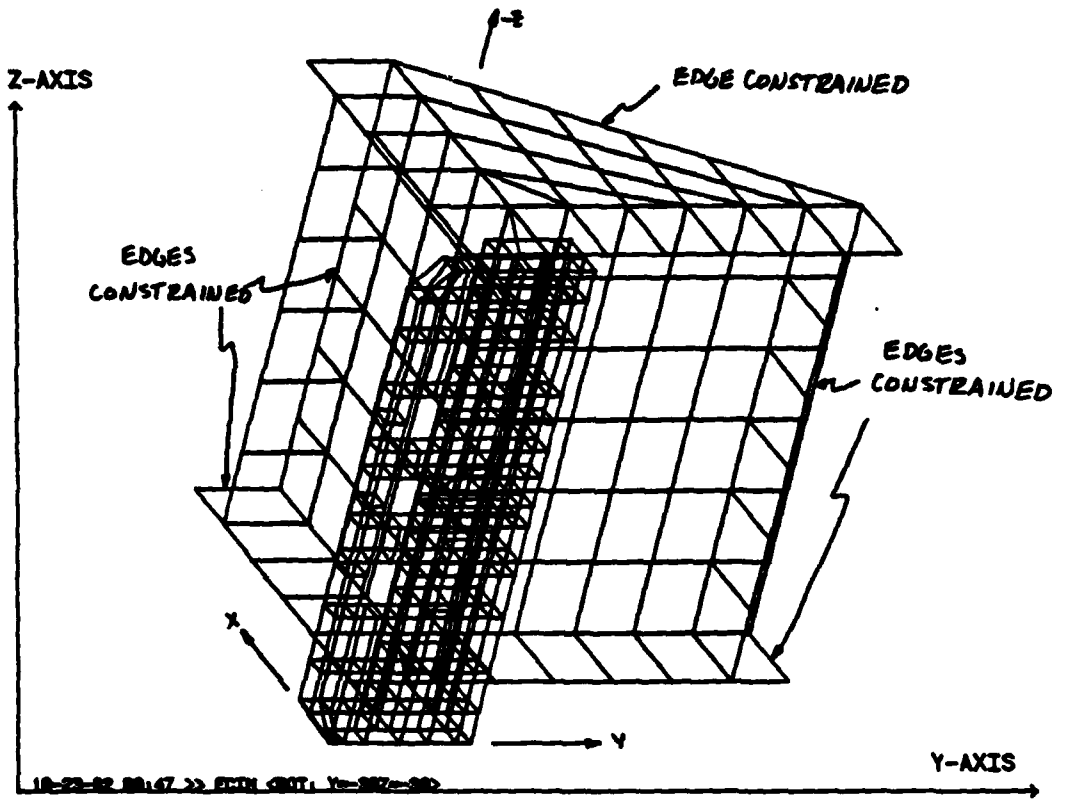


Figure 2.1.2.3-4 Rear Corner Finite Element Model

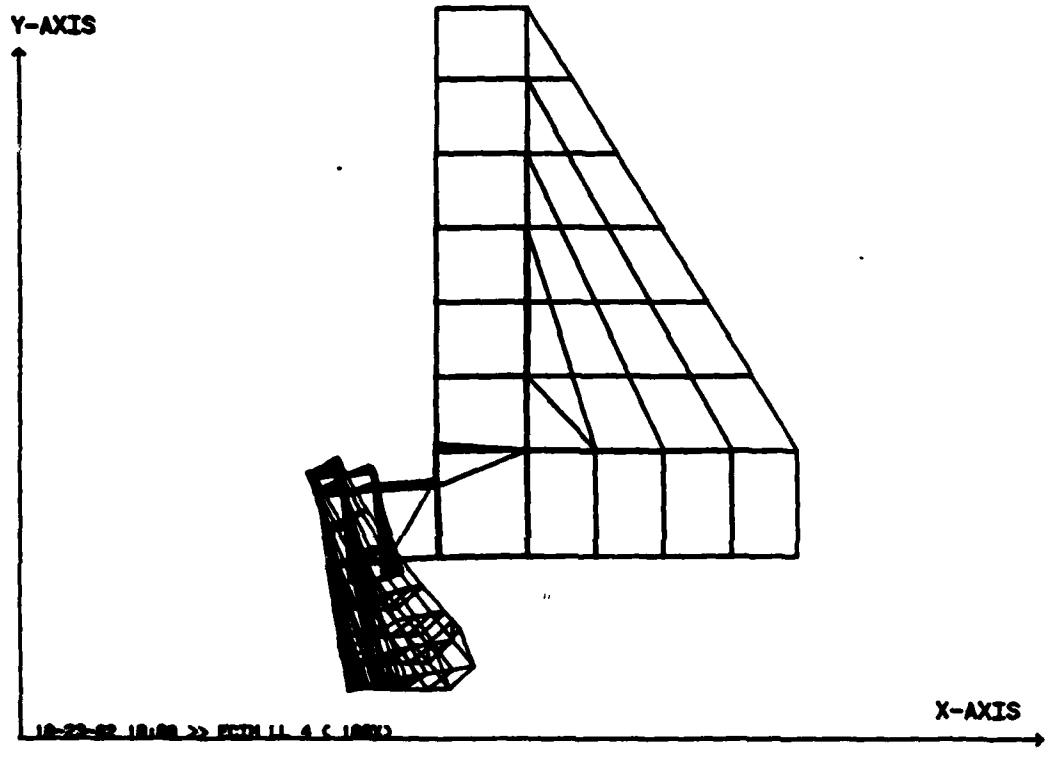


Figure 2.1.2.3-5 Rear Corner Deformation (Amplified X100)

2.1.2.4 Module Design And Layout

The mechanical design and layout of the power amplifier/power supply, splitter, combiner, attenuator and EMI filter have been completed. Final layout and detail design of the low pass filter/coupler, RF driver amplifier, driver amplifier power supply, and control module are in process.

The overall design concept of the modules remains as originally proposed. The modules plug into an interconnecting printed circuit board and are bolted to the main case, providing a direct thermal path to the case exterior.

2.1.2.5 Fabrication Of Main Case And PA Heat Exchanger

Design and detail drawings of the main case and power amplifier heat exchanger modules have been completed. Drawings were submitted to four sand-casting vendors for fabrication quotation of the main case and to two vendors for the investment-cast heat exchangers. ECI Engineering surveyed four of the potential vendors.

The order for the main case has been placed with Armstrong Molding, Syracuse, N.Y. The power amplifier heat exchanger order has been placed with Ceremet, Inc. of Allentown, P.A.

Rather than attempt to describe the details of the main case and power amplifier heat exchanger, copies of the actual drawings are shown in Figures 2.1.2.5-1 thru 2.1.2.5-6 for review.

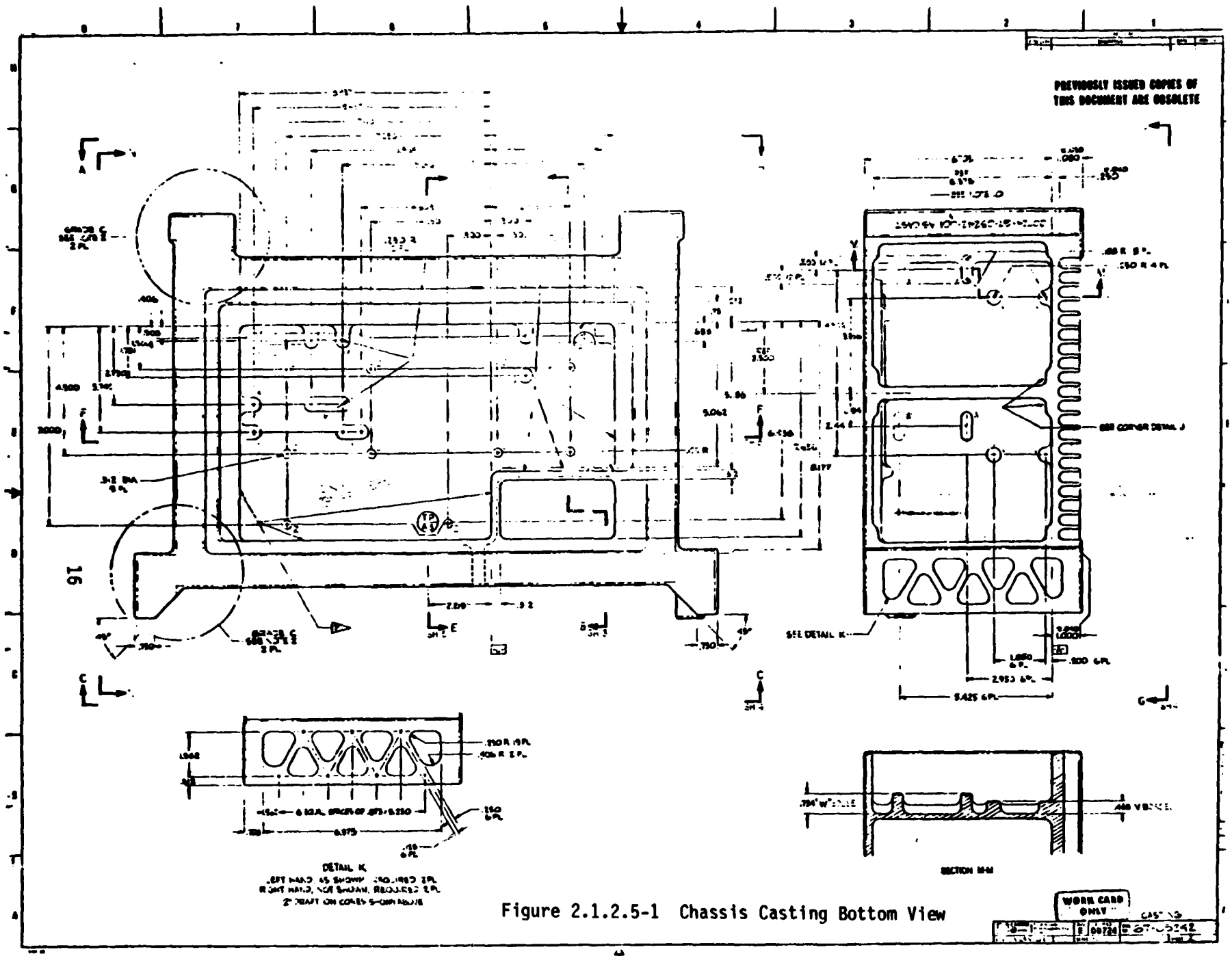


Figure 2.1.2.5-1 Chassis Casting Bottom View

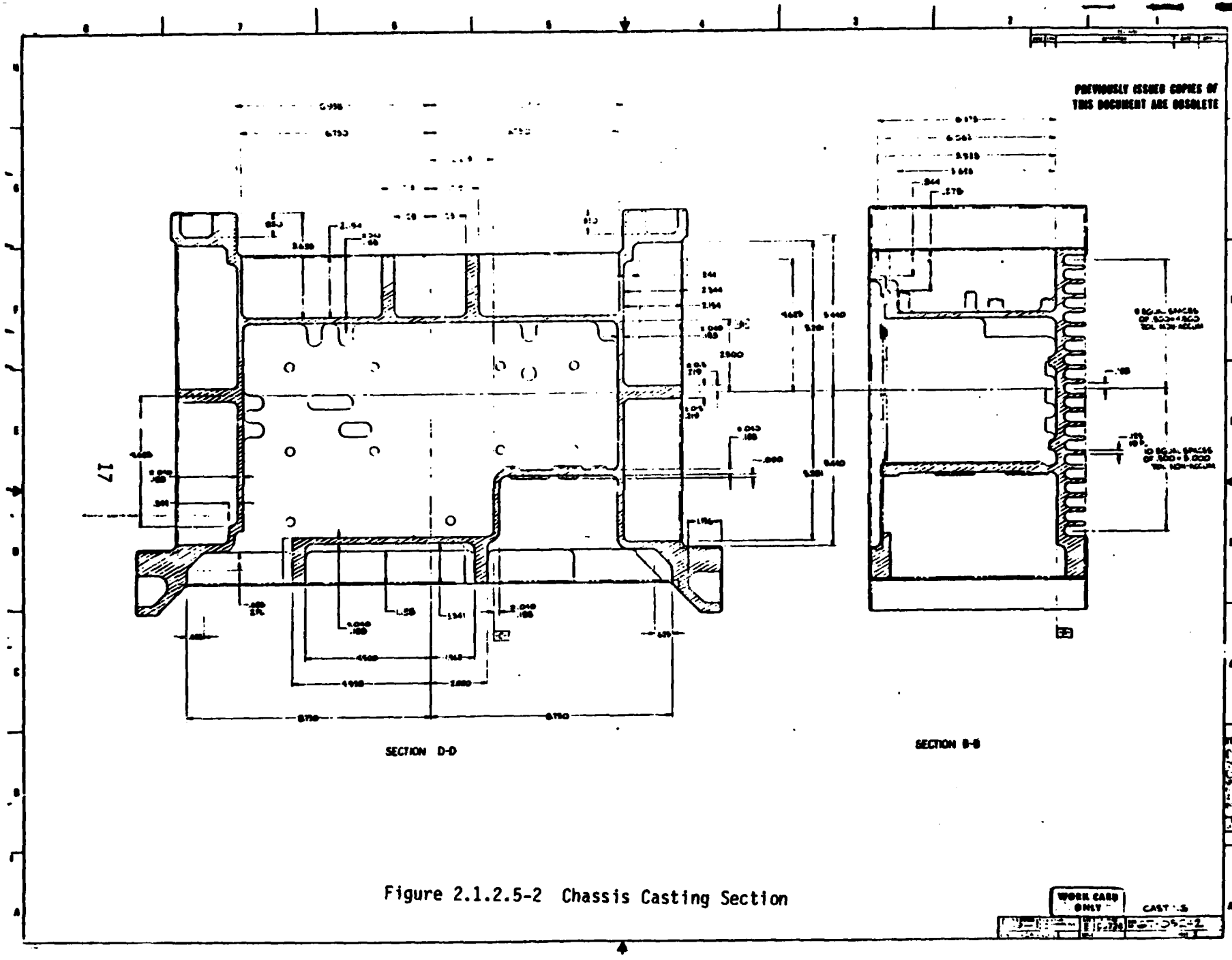


Figure 2.1.2.5-2 Chassis Casting Section

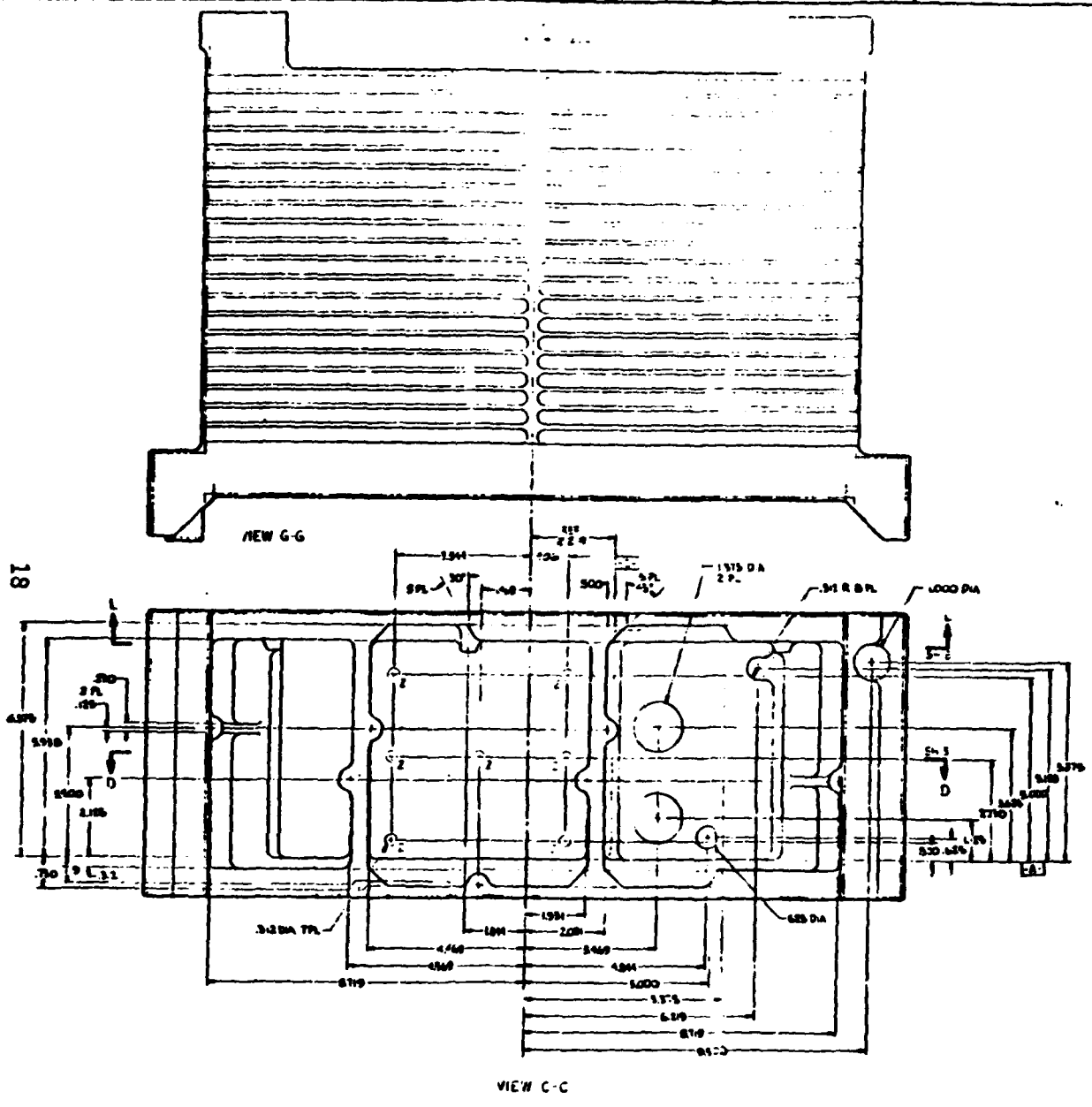


Figure 2.1.2.5-3 Chassis Casting Top and Front Views

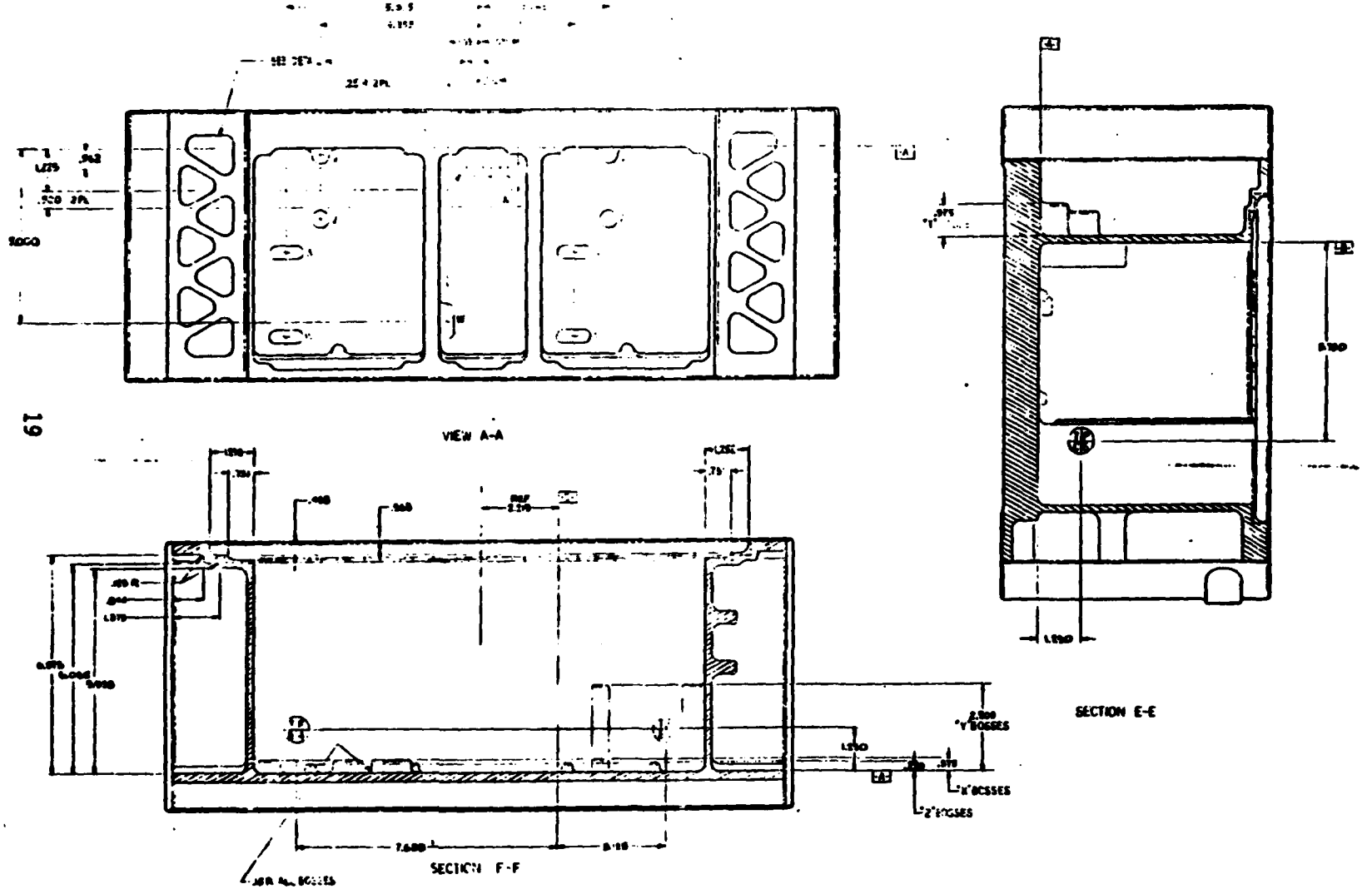


Figure 2.1.2.5-4 Chassis Casting Rear View

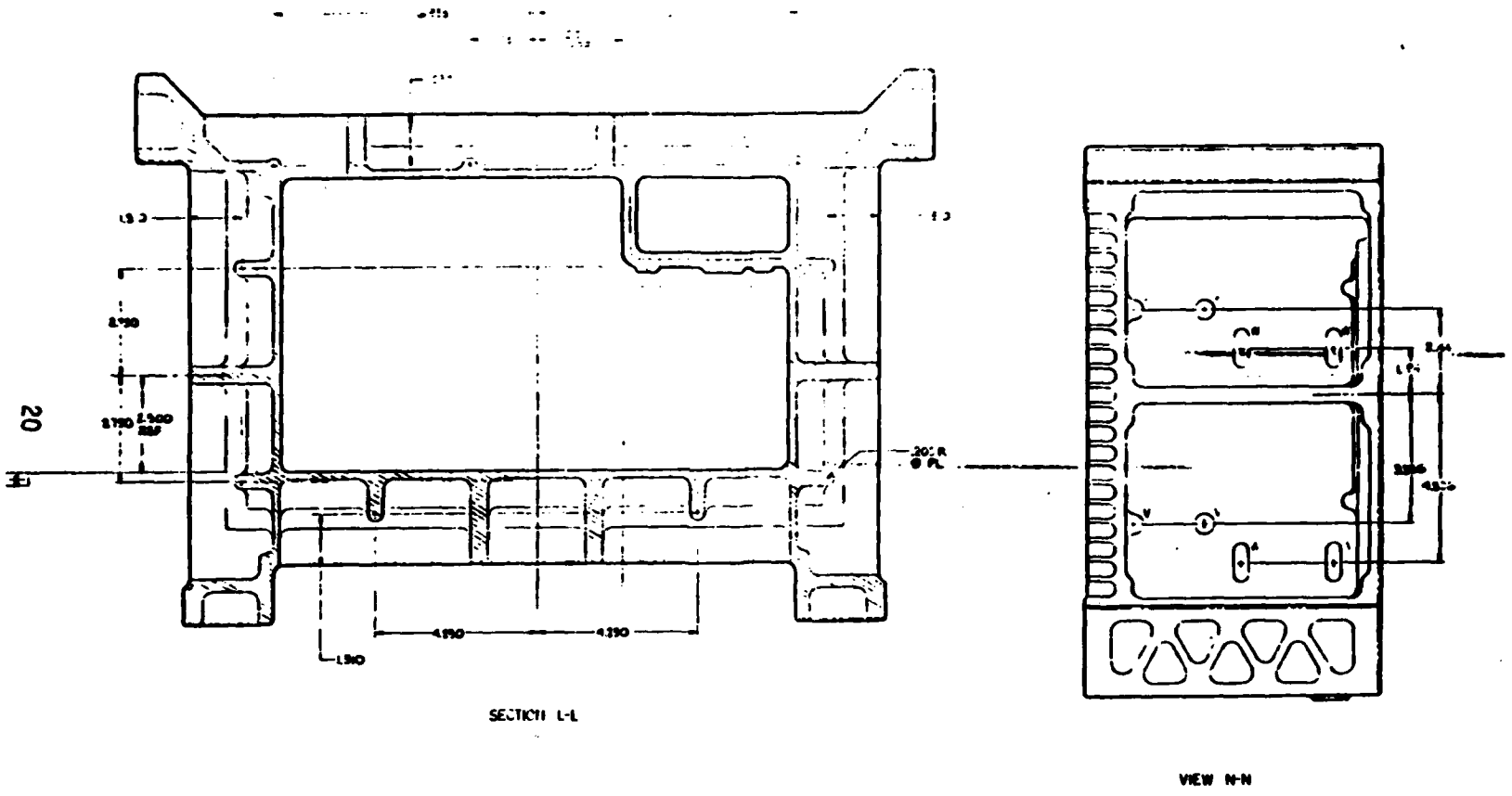


Figure 2.1.2.5-5 Chassis Cross-Section View

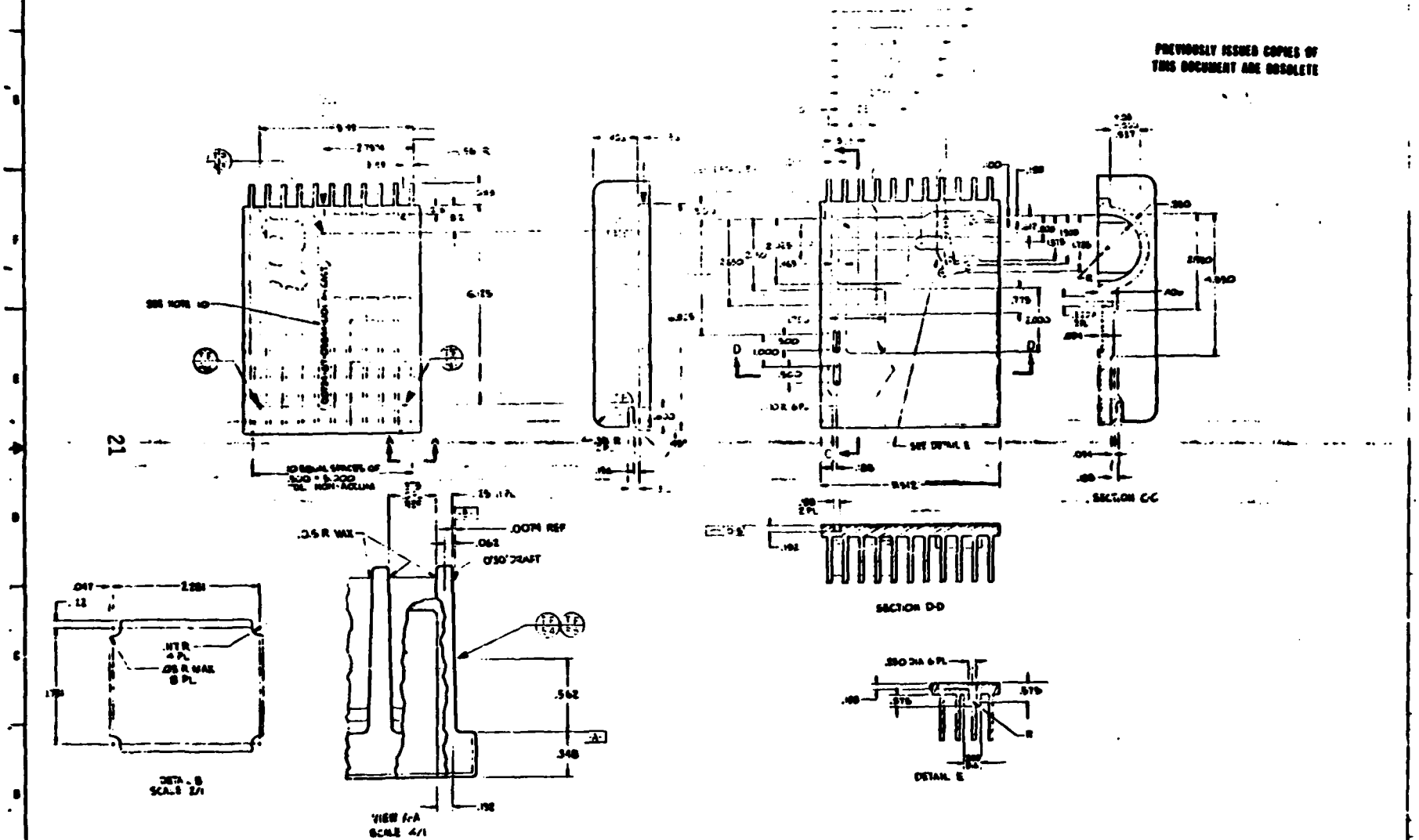


Figure 2.1.2.5-6 Amplifier Module Casting

2.2 POWER AMPLIFIER SUBASSEMBLY (CHASSIS) (A1)

In addition to providing a housing and heatsinking for the internal amplifier modules, the power amplifier chassis contains the electrical interconnect motherboard and RF cabling as well as the primary power input circuit and EMI filter.

Figure 2.2-1 is a schematic of the primary power input circuit. The DC primary input voltage is first passed through a 150-amp circuit breaker to protect the vehicle power supply from amplifier failures. A low-power, high-voltage spike supressor (VR1) next clips any high-amplitude, low-energy spikes from the vehicle supply. The input current is then switched by a power contactor (K1), then again limited by a high-power, low-voltage surge supressor. An EMI filter provides filtering to internal power supply switching transient signals.

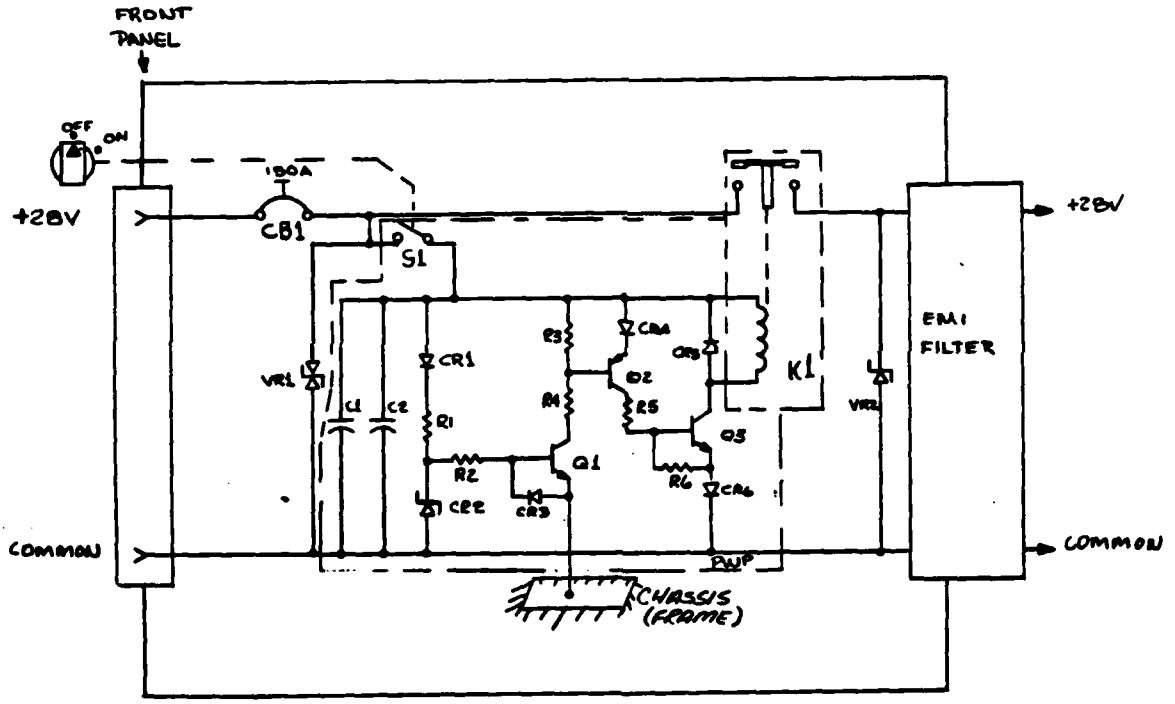


Figure 2.2-1 Primary Power Input Circuit

The power contactor is controlled by the front panel switch (S1) and includes a circuit to insure that the chassis is connected to the input return line (as it normally is in vehicular installations). This circuit passes a small bias current through the safety ground to enable a pass transistor in the power contactor coil circuit. The input primary lines are otherwise totally isolated from the case in this and all other modules. This scheme provides both reverse polarity protection and operator safety under all combinations of possible fault conditions.

The emitter of Q1 is connected directly to the chassis or frame of the amplifier. An external connection between the amplifier chassis and the vehicle frame strap must be present to bias Q1 on. This circuit in turn closes the 200-amp relay (K1) by subsequent conduction of Q2 and Q3. The current used to sense the connection of the chassis to the vehicle frame is less than 5 milliamps. Diodes CR1, CR3, CR4, and CR6 prevent the relay from energizing when there is a polarity reversal of the primary input power and provide transient protection for the transistors.

A breadboard circuit of the relay controller has been evaluated and no problems are anticipated.

The motherboard mechanical and electrical designs are presently in progress.

2.3 BITE/MONITOR (A2)

The A2 BITE/Monitor module (Figure 2.3-1) is controlled by an 8-bit Intel 8085 microprocessor. The processor clock is derived from the 16 MHZ master oscillator. The RAM, a timer and the parallel I/O ports used are built into a companion LSI chip (an 8155). In order to reduce noise in the system, the microprocessor data bus does not leave the processor board. All digital input and output to the other modules is done through a bidirectional port enabled only when the processor needs to communicate with external modules. Selects for the ports on the other modules are also generated through output ports to reduce noise.

The front panel output power and display control switches are read continuously by the processor, and the three-digit LED front panel displays are updated when there is a change in the displayed data or whenever an error occurs. An "E" followed by a two digit error code is displayed to help the user isolate the error to a module or an external source.

An 8-bit digital-to-analog converter with a buffer amplifier on the processor board drives comparators on the other modules. The comparator output is fed back to the processor where a successive approximation algorithm is executed to determine the actual voltage being sensed when the level is outside the expected predetermined boundaries.

The schematic diagram of the clock-generating circuits is shown in Figure 2.3-2. From a 16 MHz crystal-controlled oscillator, the following outputs are generated: (1) 5.333 MHz for the processor, (2) the clear and gate signals for the frequency counter (Module A7), and (3) the eight-phase power supply clock. A 5.333 MHz signal for the processor is generated by connecting a NOR-gate to dual D-type, positive-edge-triggered flip-flops as shown in the schematic. This configuration yields a divide-by-three counter with a 33 percent output duty cycle. The flip-flops must be very fast in order to insure that the output of the NOR-gate is set-up before the leading edge of the clock pulse. Therefore, a 54S74 is used in this circuit. The divide-by-three circuit

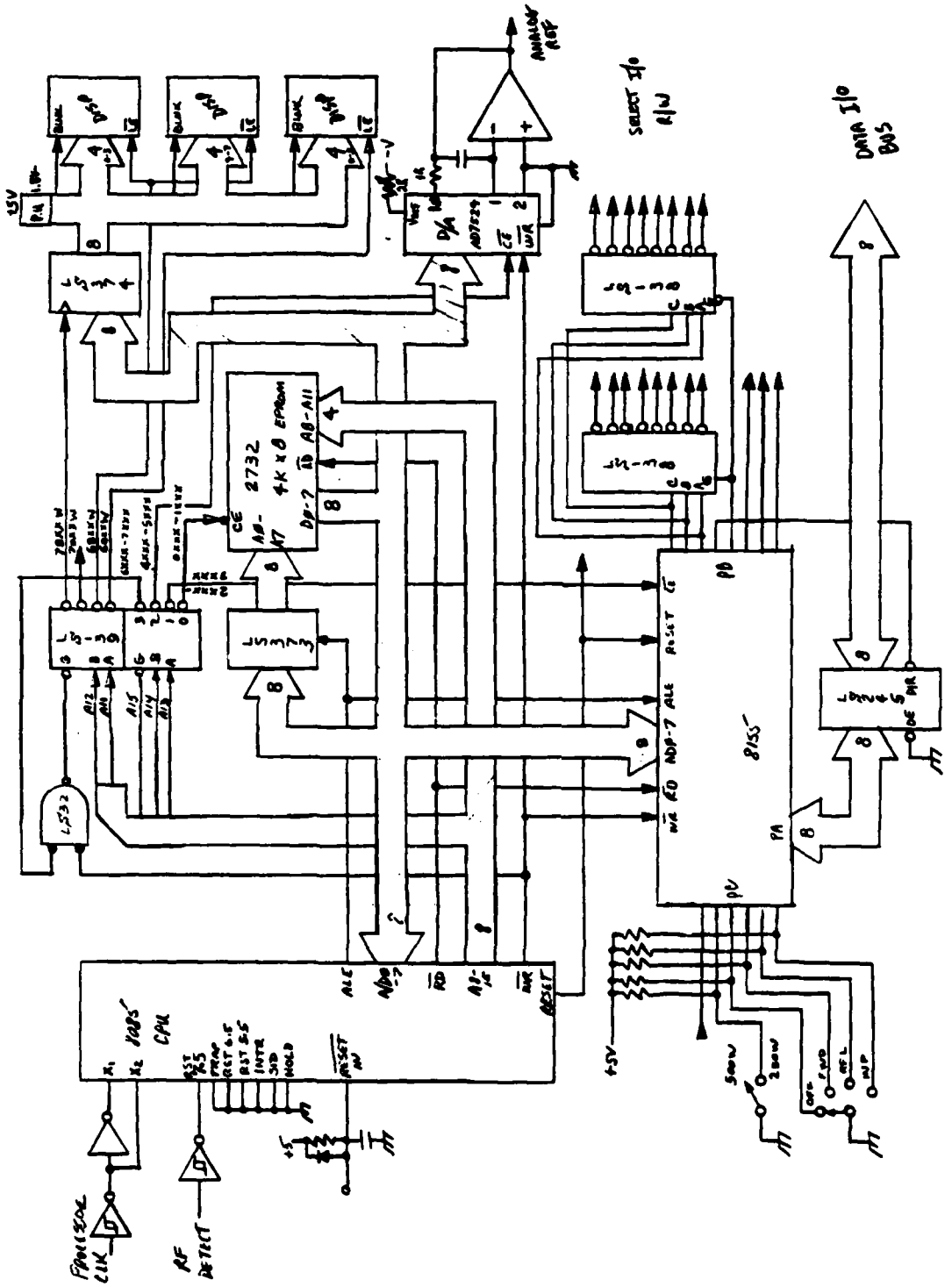


Figure 2.3-1 [illegible]TE/Monitor Circuit Schematic

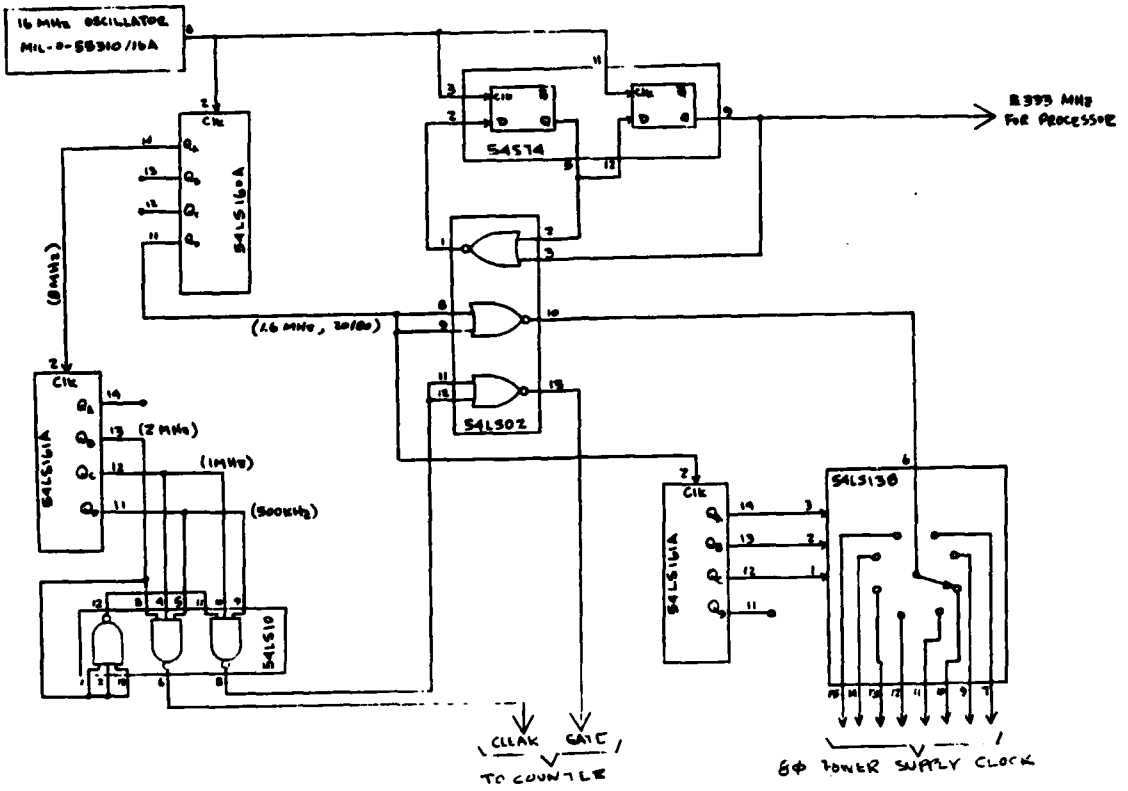


Figure 2.3-2 Power Amplifier Clock Circuits

is self-starting as shown in the state diagram (Figure 2.3-3). The frequency counter clear and gate pulses are described in Section 2.8.2 of this report. The power supply clock output is as shown in the timing diagram of Figure 2.3-4.

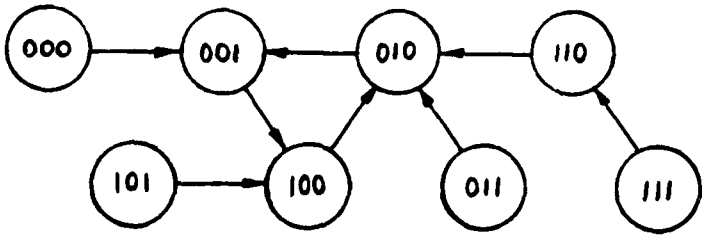


Figure 2.3-3 Divide-By-Three State Diagram

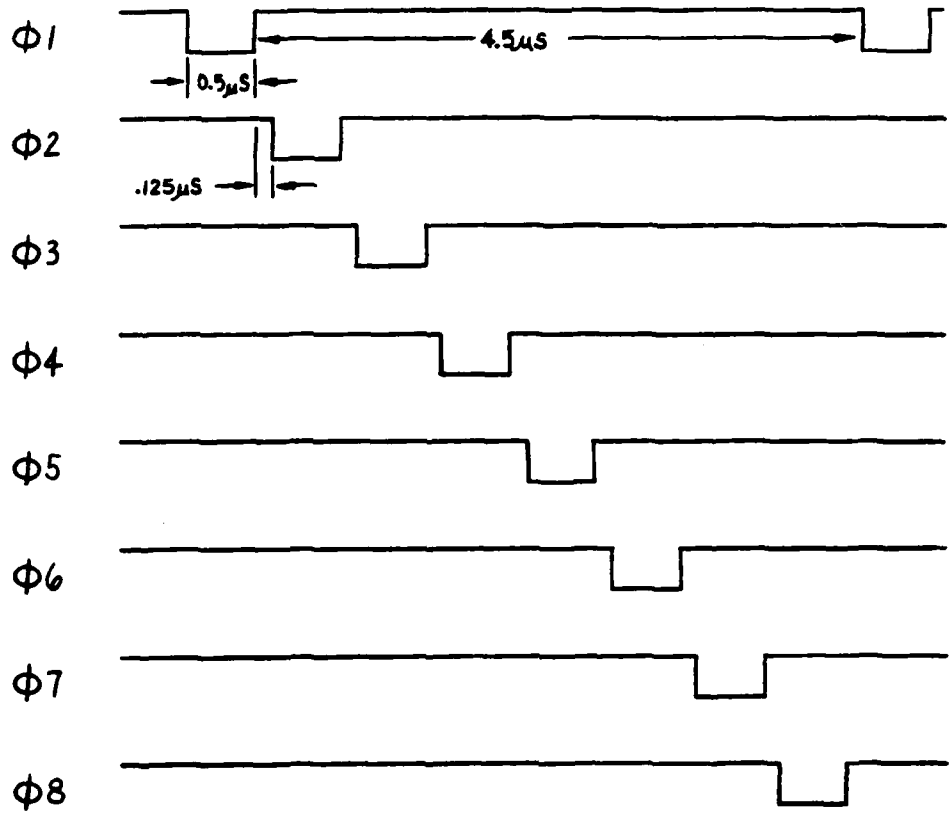


Figure 2.3-4 Power Supply Clock Output

Development of the final amplifier functional flow chart is not complete at this time. Therefore, final completion of the amplifier controller circuits has not been accomplished, and generation of control software beyond a few standard self-check routines has not begun. As soon as all amplifier functions are documented and self-protection output power levels are determined, this effort will be restarted.

2.4 COAX RELAY/RF BYPASS (A3)

The coax relay/RF bypass module is an electromechanical RF relay bypass of the power amplifier to provide an interconnection between the driving transmitter and the output antenna when the power amplifier is unpowered or if a system failure prevents normal operation. The module includes an RF input coaxial relay, high power vacuum RF output relay, a bypass line detector and a relay driver circuit.

The input relay is a sealed SPDT relay with coaxial terminations capable of switching up to 70 watts of RF "hot" and 200 watts "cold". Because of the power level and equipment explosion requirements, a vacuum relay is used in the RF output line. A simple resistively-tapped diode detector is installed in the bypass line to signal the presence of an RF drive signal so that the relays can be commanded to switch only when drive is not applied. An integral drive circuit interfaces the relay coil drive current to a low level control circuit.

Figure 2.4-1 is a schematic of the coax relay bypass assembly. The de-energized conditions of relays K1 and K2 allow conventional transceiver operation when the amplifier is unpowered or when the relays are de-energized by the system controller. When drive is present with the

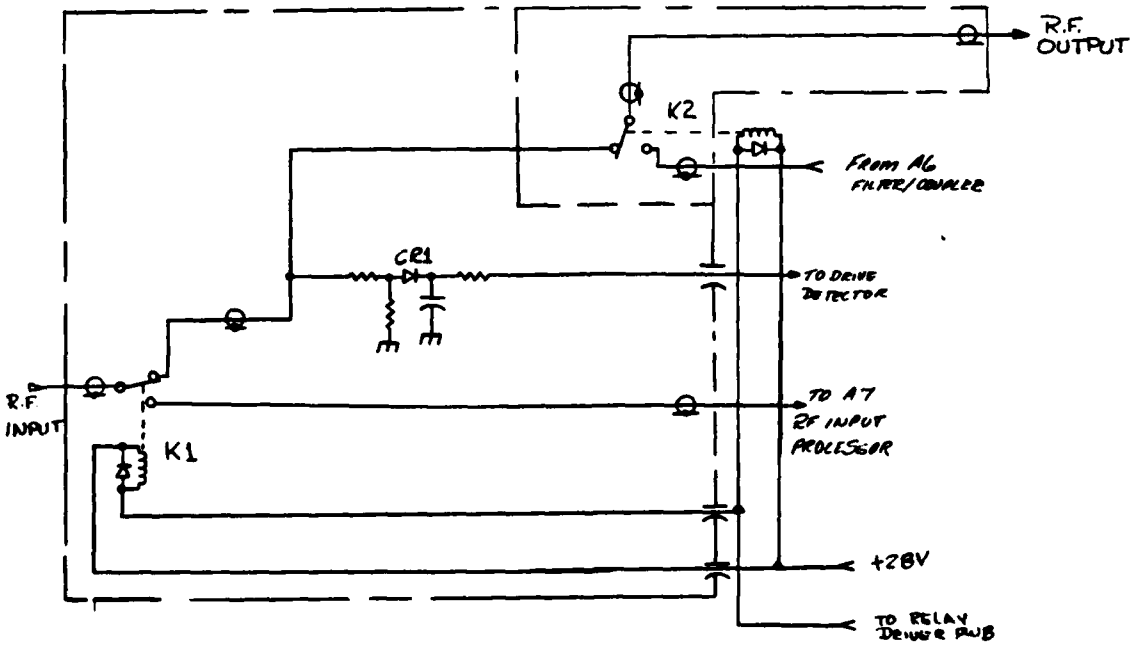


Figure 2.4-1 Coax Relay Bypass Circuit Schematic

relays de-energized, a voltage is developed by the resistively-tapped drive detector (CR1) and sensed by the comparator (U1) on the detector and driver assembly. If drive is present, the comparator transmits a logic zero to the system processor.

The two armatures of relays K1 and K2 are driven in parallel by the relay driver (Q1) as shown in Figure 2.4-2. A high impedance presented by the system controller to the base of Q1 allows bias to be applied and forces Q1 into conduction. A ground applied to Q1 removes the bias and Q1 is placed into cutoff, turning off the relays.

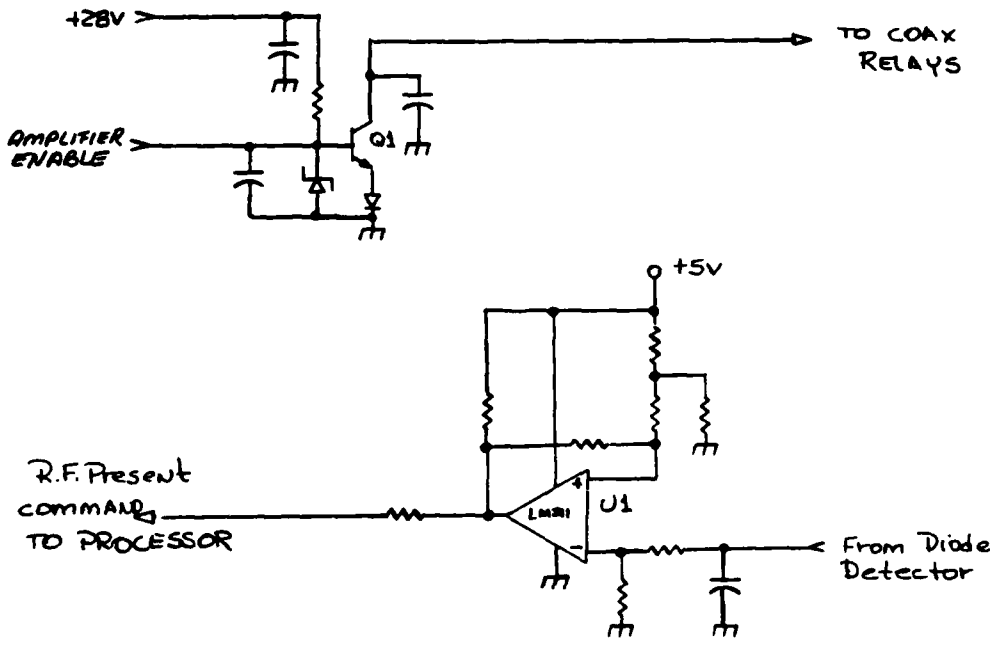


Figure 2.4-2 Power Detector And Relay Driver Schematic

2.5 POWER INPUT ASSEMBLY (A4)

The power input assembly is a front panel mounted circuit that is the initial interface to the amplifier primary power source. The assembly contains only three major parts: the input power connector, the power control switch, and the input 150-amp circuit breaker. The components in this module connect to the power relay, transient protectors, and EMI filter of the chassis.

The input power connector is a MS90558N44NO3P military part rated at 100 amps. This connector is polarized and designed for 28-volt DC applications. A two position rotary switch is used to enable primary power to the amplifier. The power input assembly exists as a packaging convenience, and the associated circuits are described in Section 2.2 of this report.

2.6 POWER SYSTEM DEVELOPMENT

The DC power system required for the 500-watt power amplifier consists of eight separate switched-mode power converters. Six of the converters are identical and are used to provide power to each of the six RF output amplifiers. These converters contain two outputs: a high current (9 amps max) 28-volt output and a low current (0.9 amps max) 4-volt output.

A seventh converter used to power the RF drive circuit, while very similar to the first six, contains only one 28-volt, 5-amp (max) output. The eighth converter, on the otherhand, contains multiple outputs and is used to provide power to the various control, monitor, BITE, and primary power supply control circuits.

A block diagram of the entire DC power system is shown in Figure 2.6-1, and Table 2.6-1 lists the DC requirements of each converter. Figures 2.6-2, 3, and 4 show block diagrams of each of the three types of converters used in the system. Note that the input source lines are DC isolated from the converter outputs through transformer coupling and separate ground returns to minimize chassis currents.

Inherent in each of the converters is the generation of large input ripple currents at the switching rate and its harmonics. The total current exhibited on the input source lines must be reduced below that specified in MIL-STD-461A, Notice 4 (tailored) under conducted narrowband emissions for DC and interconnecting leads. Figure 2.6-5 illustrates this requirement in the frequency range of 10 kHz to 100 MHz.

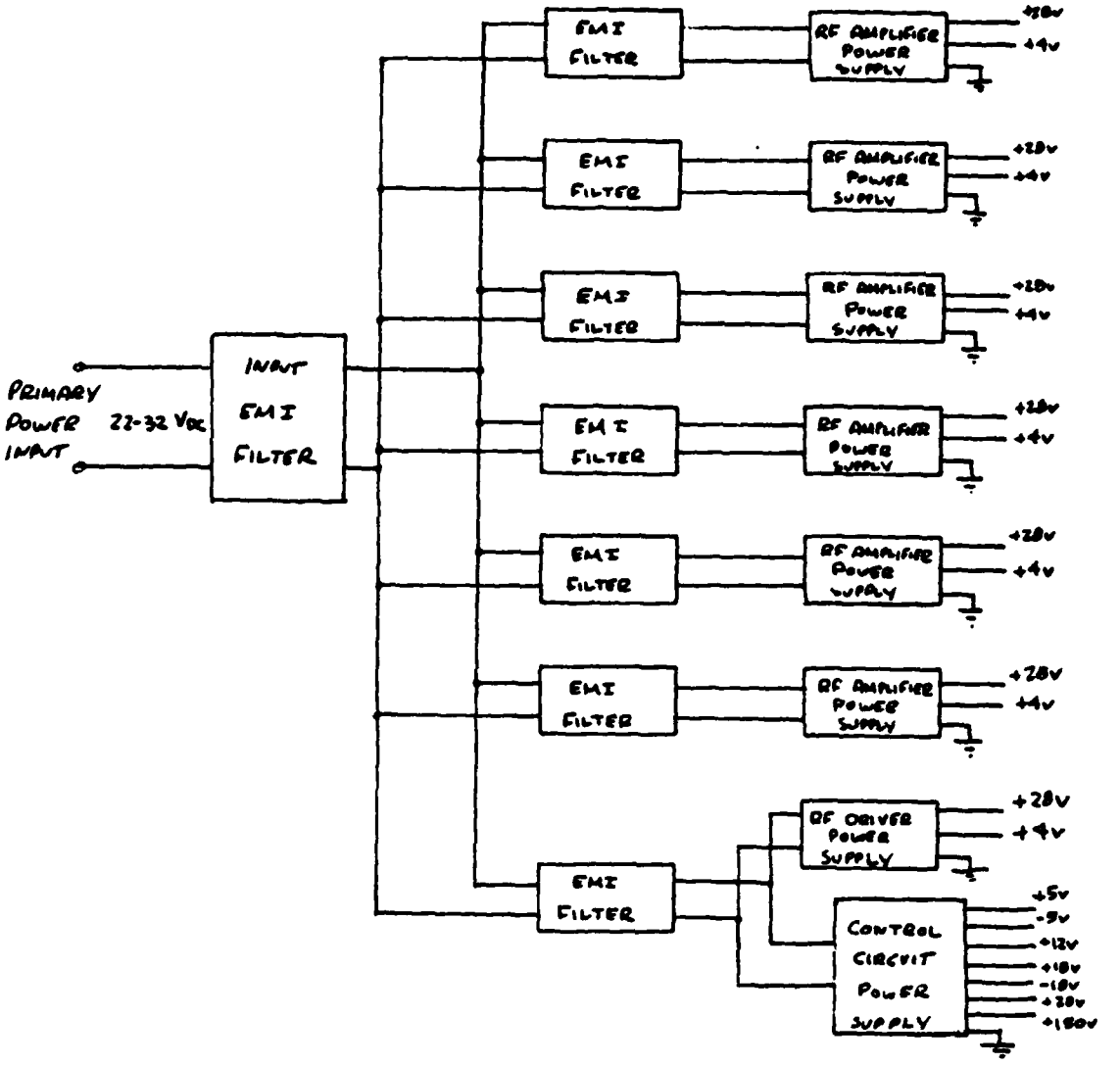


Figure 2.6-1 DC Power System Block Diagram

Table 2.6-1 Power Converter DC Requirements

	MINIMUM	TYPICAL	MAXIMUM	UNITS
CONTROL CIRCUIT POWER SUPPLY				
DC OUTPUTS				
1. Logic Supply				
DC Voltage	4.75	5.0	5.25	Volts
Ripple Voltage			0.1	Volts
DC Current			3.5	Amps
2. PIN Diode Forward Bias Source				
DC Voltage	-6	-5	-4	Volts
Ripple Voltage			20	mVolts
DC Current			3.0	Amps
3. PIN Diode Reverse Bias Source				
DC Voltage	130	150	170	Volts
Ripple Voltage		2	5	mVolts
DC Current			2	mAmps
4. Control Circuit Positive Source				
DC Voltage	17.5	18.5	20	Volts
Ripple Voltage			50	mVolts
DC Current			175	mAmps
5. Control Circuit Negative Source				
DC Voltage	-20	-18.5	-17.5	Volts
Ripple Voltage			50	mVolts
DC Current			175	mAmps
6. Power Supply Controller Source				
DC Voltage	8	12	15	Volts
Ripple Voltage			100	mVolts
DC Current			1.05	Amps
7. Bypass Relay Source				
DC Voltage	24	28	32	Volts
Ripple Voltage			200	mVolts
DC Current			120	mAmps
DRIVER AMPLIFIER POWER SUPPLY				
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
DC Current	0	4.2	6.0	Amps

NOTE: Current reduces linearly by approximately 0.4 dB/volt for input voltages below 27.5 volts.
Supply to include current limit circuit to fold-back at loads above 6.0 amps.

Table 2.6-1 Power Converter DC Requirements (Cont.)

	MINIMUM	TYPICAL	MAXIMUM	UNITS
OUTPUT AMPLIFIER POWER SUPPLY				
1. Amplifier DC Supply				
DC Voltage	26.5	28.0	29.5	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-90	dB
DC Current	0	7.5	9.0	Amps
NOTE: Current reduces linearly by approximately 0.4 dB/volt for input voltages below 27.5 volts. Supply to include current limit circuit to fold-back at loads above 9.0 amps.				
2. Bias Source Supply				
DC Voltage	3.6	4.0	4.4	Volts
Ripple (Components to 1 MHz)			-20	dB
Ripple (Components above 1 MHz)			-60	dB
DC Current	0.01	0.3	0.9	Amps
NOTE: Bias source load is directly proportional to the output supply load.				

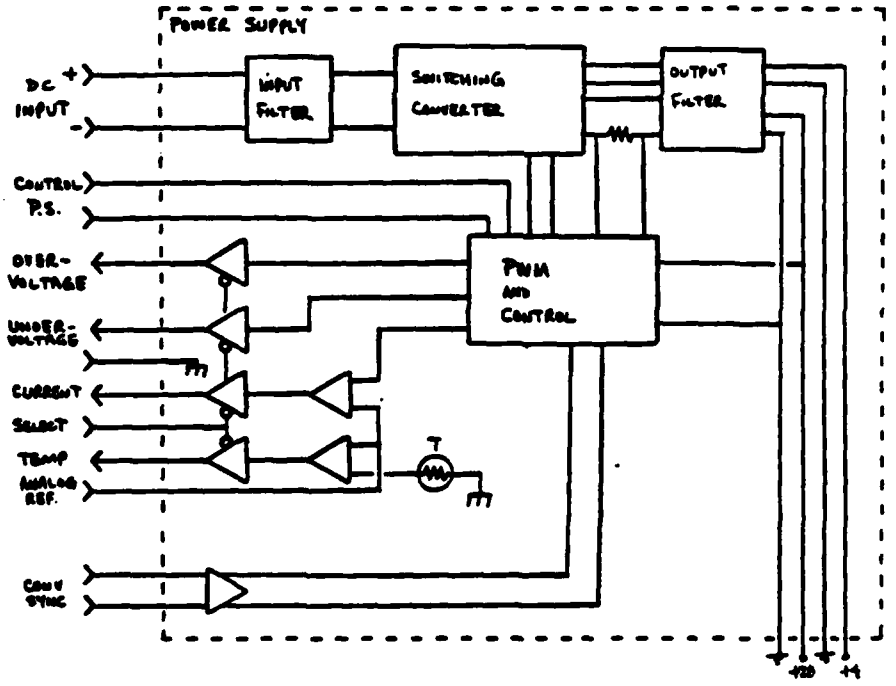


Figure 2.6-2 RF Amplifier Power Supply Block Diagram

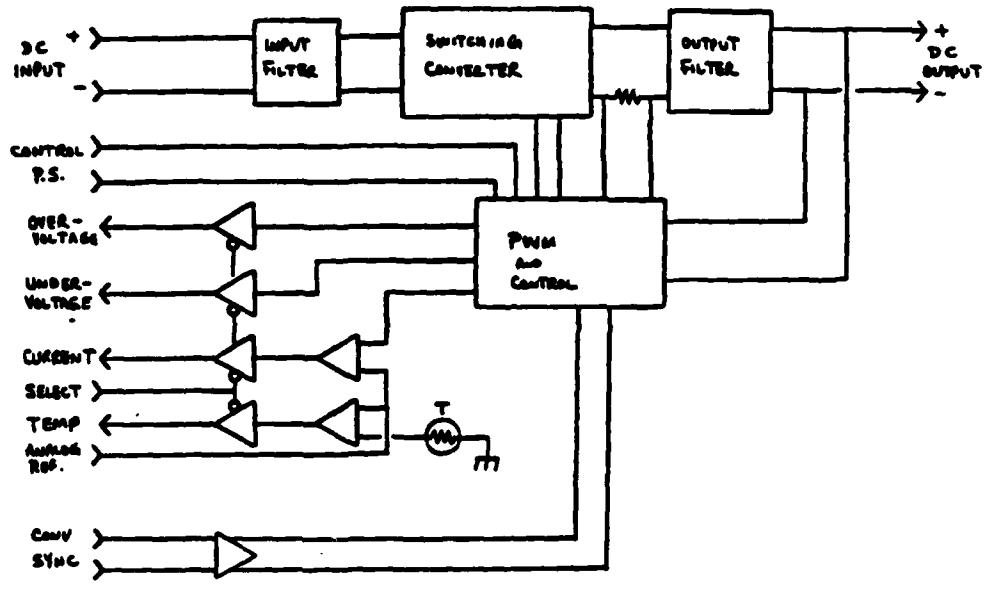


Figure 2.6-3 Driver Amplifier Power Supply Block Diagram

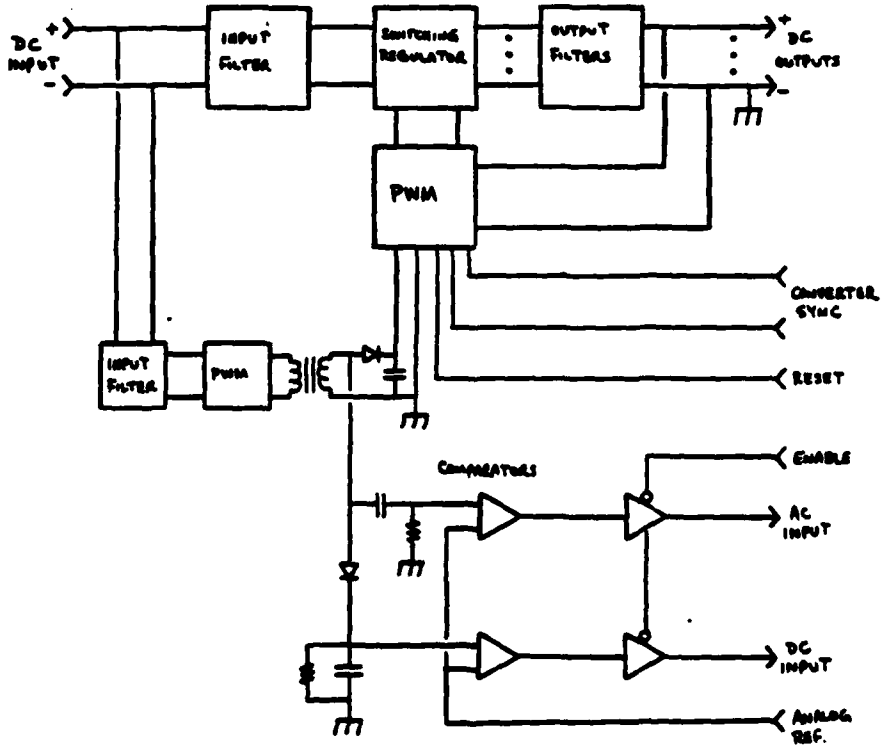


Figure 2.6-4 Control Circuit Power Supply Block Diagram

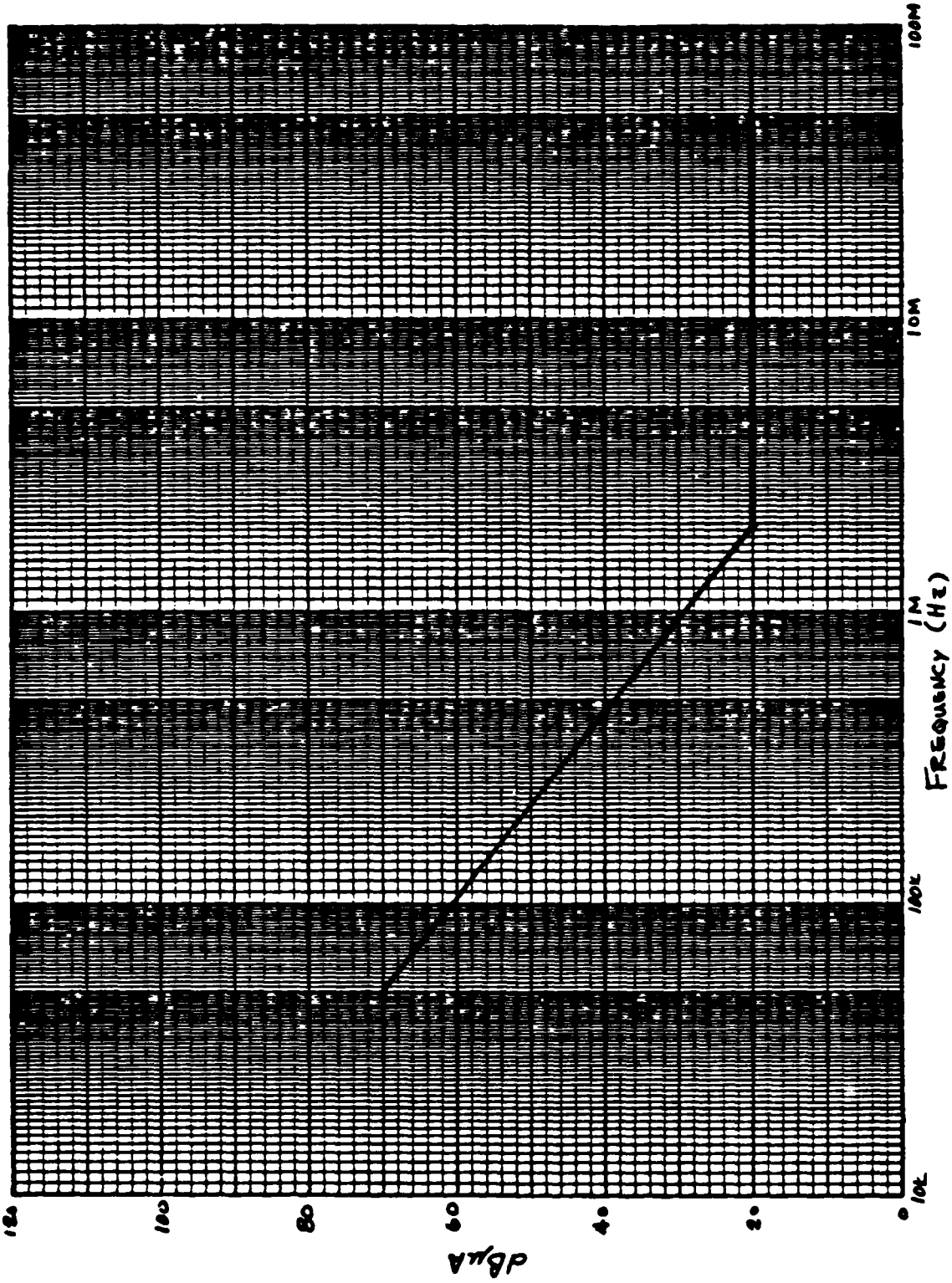


Figure 2.6-5 Power Converter Input Filter Requirements

Attenuation to converter currents is accomplished primarily with L-C type low pass filter sections. In addition, the eight converters will be synchronized to a master clock, each phase-staggered relative to the others, so that peak currents are kept to a minimum.

The 28-volt DC input to the power system will originate from a 28-volt military vehicle power supply as characterized in MIL-STD-1275A. While the DC voltage of the vehicle supply will lie within 22-32 VDC, numerous transients may be exhibited depending on the supply condition. Three "commonly occuring" conditions exist: Fault-free including (1) combined generator-battery supply or (2) battery-only supply, and single-fault including (3) generator-only supply. An uncommon event is a multiple-fault condition where both the battery and generator regulator fail. The supply characteristics under all these conditions are listed in Table 2.6-2.

In order to protect the equipment from damage due to power supply transients, a 105-volt spike suppressor and a 34.5-volt surge suppressor will be placed ahead of all circuitry. These devices will not protect against the 14V p-p ripple voltage under single-fault conditions, however, and design of the power system must address this "commonly" occurring condition.

During this report period both the control circuit power supply and the RF amplifier power supply have been breadboarded and evaluated with the results included in Section 2.6.1 of this report. EMI filter elements and configurations have been selected and their effects on individual converter performances simulated through extensive computer modeling.

Table 2.6-2 Power Source Characteristics

	GENERATOR BATTERY	BATTERY ONLY	SINGLE FAULT	MULTIPLE FAULT
Steady-State Voltage[1] (V)				
Max	30	27	33	100
Min	25	20	0	0
Ripple (Figure 2.6-6)				
Peak Voltage (+ and -) (V)	2	2	7	-
Frequency Range (Hz)	50-200 k	50-200 k	50-200 k	-
Surges				
Voltage (V)				
Max	40	100	100	-
Min	18	15	15	-
Impedance (mohms)	20	500	500	-
Figure No.	2.6-7	2.6-8	2.6-8	-
Spikes				
Peak Voltage (+ and -) (V)	250	250	250	-
Figure No.	2.6-9	2.6-9	2.6-10	-
Starting Disturbances				
Initial Engagement				
Min. Voltage (V)	6	6	-	-
Max. Time (Sec.)	1	1	-	-
Cranking Level				
Min. Voltage (V)	16	16	-	-
Max. Time (Sec.)	30	30	-	-

Note 1. Equipment-specified operating voltage limits are 22-32 VDC, 27.5 VDC nominal.

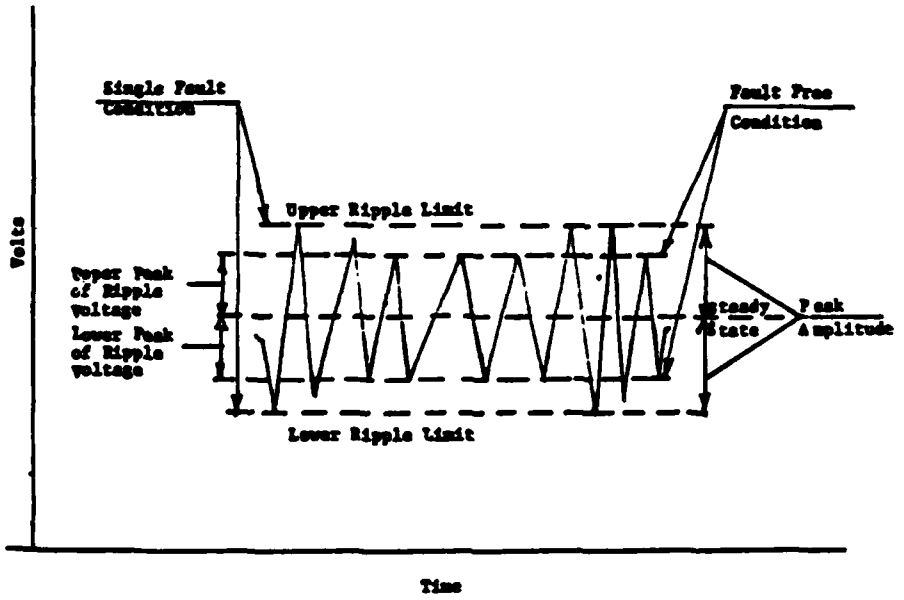


Figure 2.6-6 Ripple Voltage Definitions

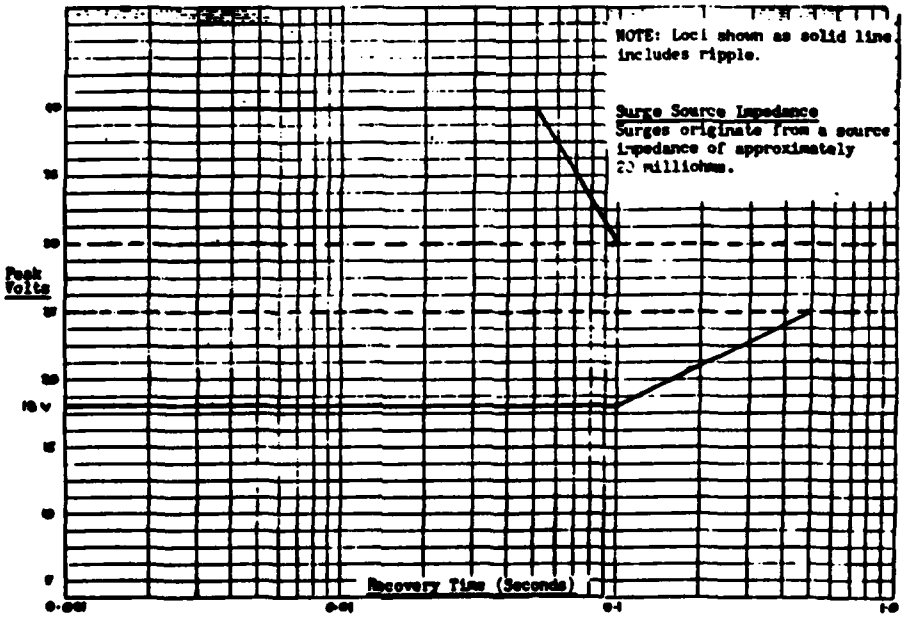


Figure 2.6-7 Surge Voltage Limits - Generator-Battery Source

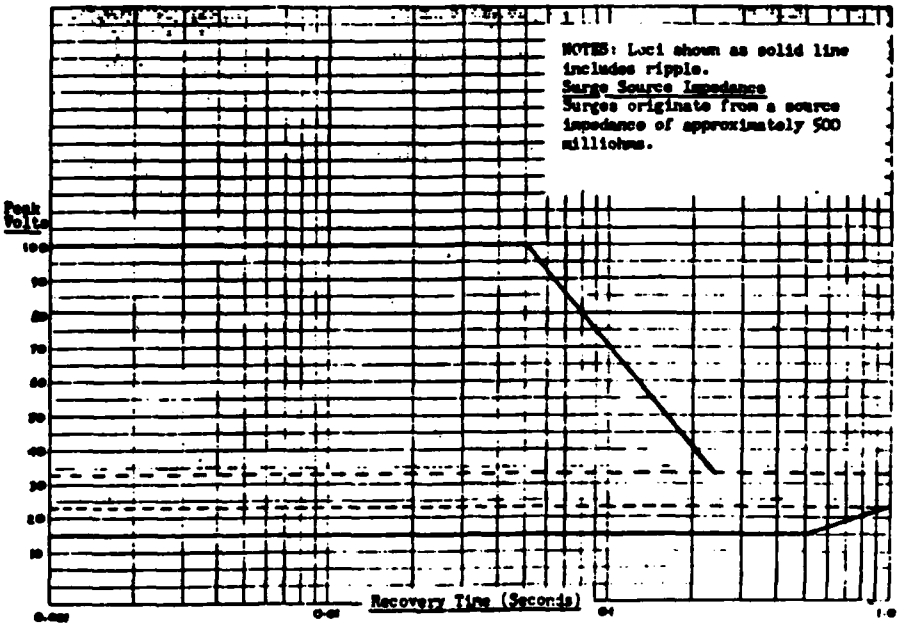


Figure 2.6-8 Surge Voltage Limits - Single-Fault Conditions

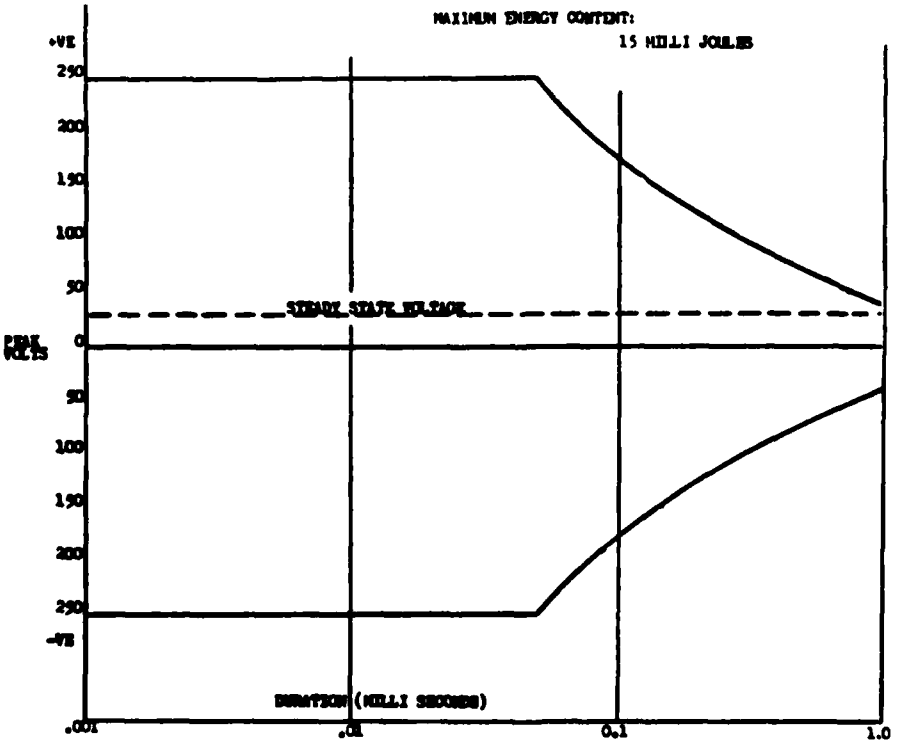


Figure 2.6-9 Spike Voltage Limits - Battery On-Line

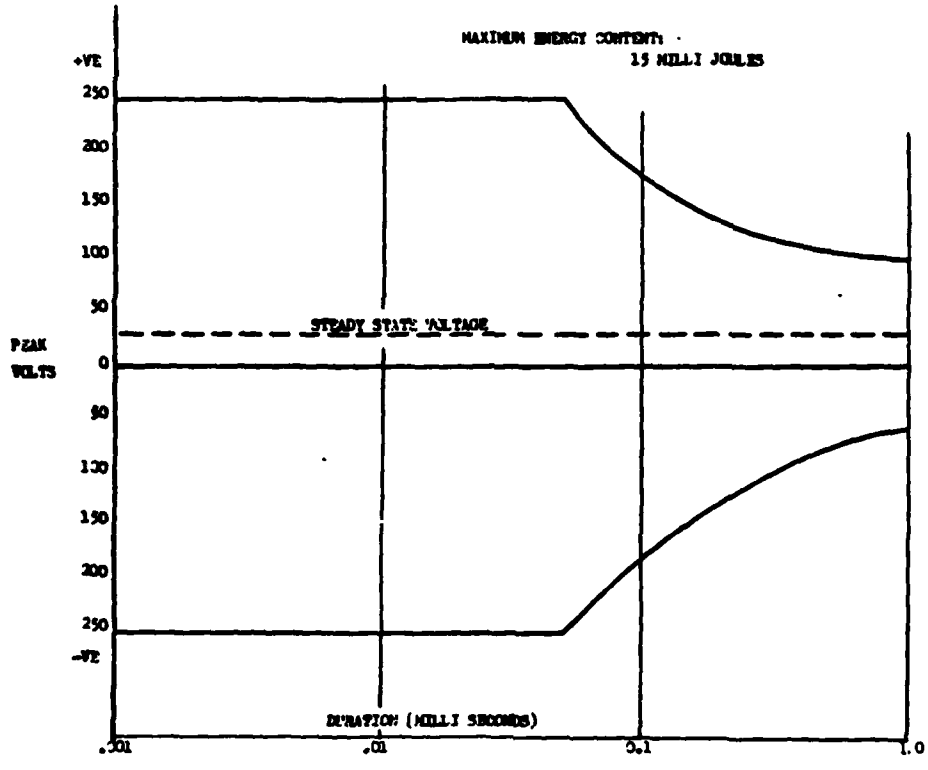


Figure 2.6-10 Spike Voltage Limits - Single-Fault Conditions

2.6.1 Power Supply Design

Requirements for the 500-watt power amplifier power supplies include:

- High efficiency
- Multiple outputs
- Minimum weight and size
- DC isolation
- Low input and output noise
- High reliability

While these goals can be achieved simultaneously to some degree through many switched-mode power supply topologies, implementation of a coupled inductor push-pull type converter can result in numerous advantages over more conventional techniques.

A schematic of the coupled inductor power converter is shown in Figure 2.6.1-1. Operation is relatively simple with the coupled inductor being its primary feature. When either transistor Q1 or Q2 is turned on, load current is supplied through transformer T1 while energy is stored in the core of the inductor L1 through its secondary winding during this period. On the next half cycle, with both transistors turned off, the voltage on the secondary winding of the coupled inductor forward biases diode D1 and load current is supplied through the coupled inductor secondary windings with the energy that was stored in the core during the previous cycle being delivered to the load. With the transistors operating in a push-pull arrangement, a complete cycle consists of each transistor exhibiting "on" periods alternately with the coupled inductor secondary supplying load current during "off" times in-between. As a result, the DC gain of this converter is given by:

$$\frac{V_o}{V_{in}} = ND \qquad (2.6.1\text{-}1)$$

Where N = Transformer and inductor turns ratio
D = Twice the duty cycle of an individual transistor

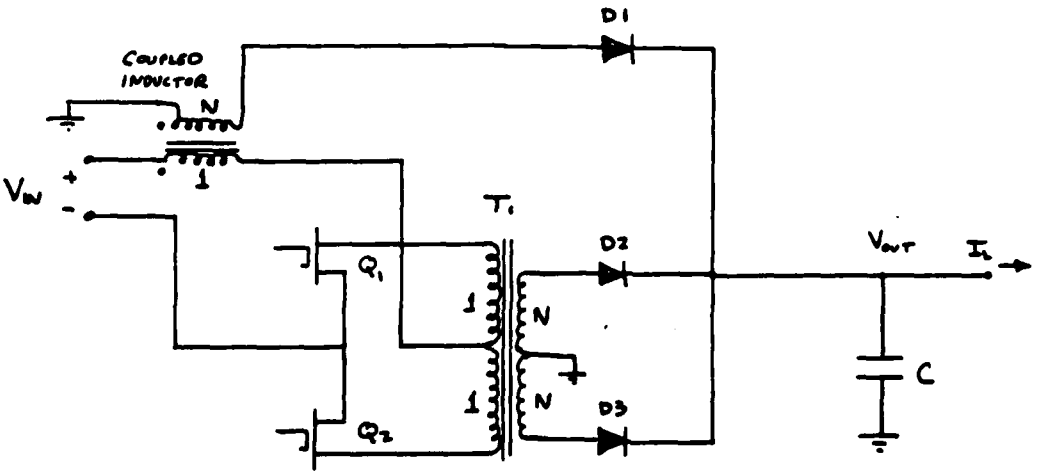


Figure 2.6.1-1 Coupled Inductor Push-Pull Converter Topology

The action of the coupled inductor leads to the primary advantages of this configuration:

- Output current is continuous, relaxing the filter requirements of the output capacitor C since the coupled inductor acts as a current source to the load at all times.

- A portion of the input voltage is dropped across the inductor primary keeping the volt-seconds applied to the transformer to a minimum and thus allowing for better core utilization and reduced diode reverse voltages.

- Rectifier diodes supply load current only during transistor "on" times since the inductor secondary supplies load current during "off" times. This situation leads to reduced average currents for these devices.

- During "on" times, the inductor primary acts as a high impedance, current-driven input circuit, thus minimizing current spikes due to rectifier recovery or transformer core saturation.

- Since all outputs are tightly coupled through the transformer during "on" times and through the inductor during "off" times, excellent cross regulation between outputs is maintained.

- Transistor voltages during "off" times are considerably reduced compared to conventional push-pull converters, allowing for lower voltage devices, reduced power dissipation during switching, and less elaborate snubber networks.

- Since the output is driven by a constant inductance on each half cycle, no right-half plane zero is incurred in the open-loop frequency response. This characteristic allows simple feedback techniques to be used.

The undesirable aspects of this converter are few in number:

- Input current is discontinuous, making EMI filter requirements greater. (Most other converter topologies result in the same current waveforms, and those which exhibit continuous current also exhibit a right-half plane zero in the open-loop transfer functions.)

- An additional rectifier is needed for each coupled output.

- Leakage reactance between the coupled inductor windings must be minimized, resulting in a complex construction. (All input and output inductors are combined on one core, however, minimizing both size and weight.)

2.6.1.1 RF Amplifier Power Supply

The amplifier power supply design is detailed by major circuit element in the following sections.

2.6.1.1.1 Power MOSFETS

A detailed schematic of the RF amplifier power converter is shown in Figure 2.6.1.1.1-1. Power MOSFETS were selected as the active devices in the push-pull network because of their fast switching times and the relatively simple gate drive circuits necessary for highly efficient operation. The drain-to-source current and voltage waveforms the devices will experience during circuit operation are illustrated in Figure 2.6.1.1.1-2. Maximum current handling, which is about 12 A rms for each device, occurs at maximum duty cycle under full load (D = 0.4, I_L = 9 A). As a result, 17-amp (T = 100°C), 100-volt IRF 140 HEXFETS were selected. Note that the gates of the MOSFETS (Figure 2.6.1.1.1-1) are transformer-coupled to the PWM IC to maintain DC isolation of the power supply input to output.

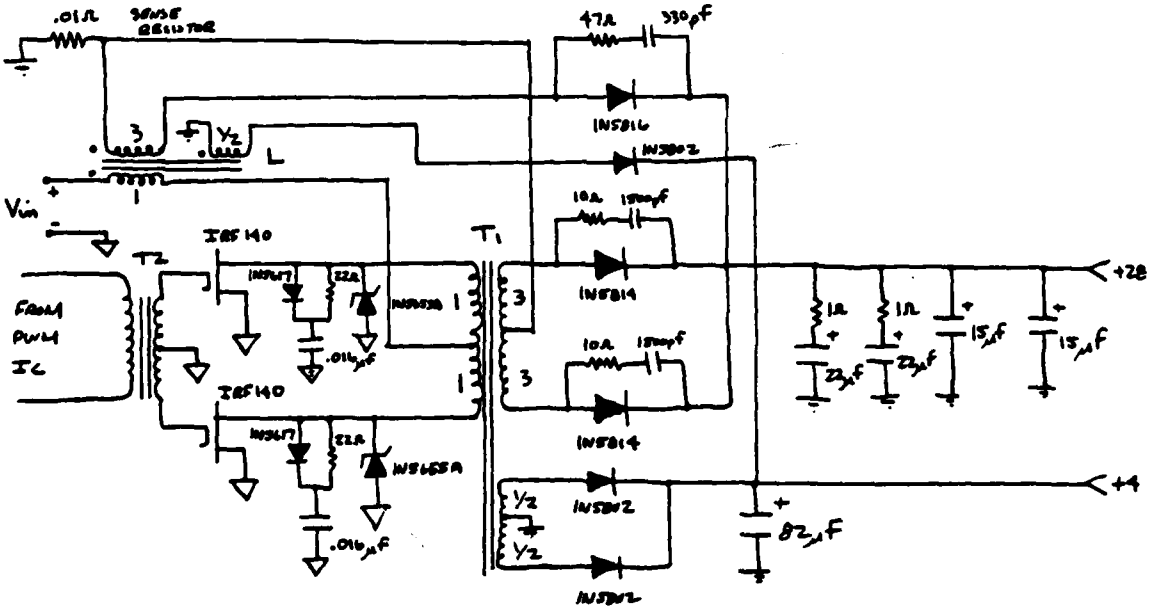
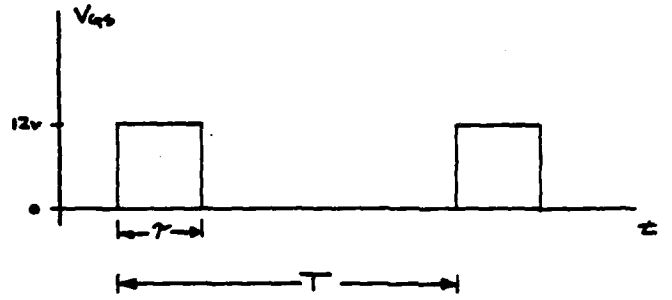
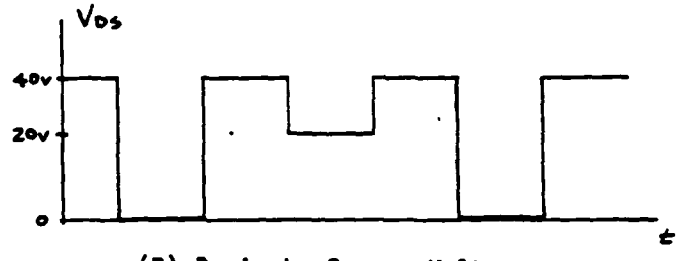


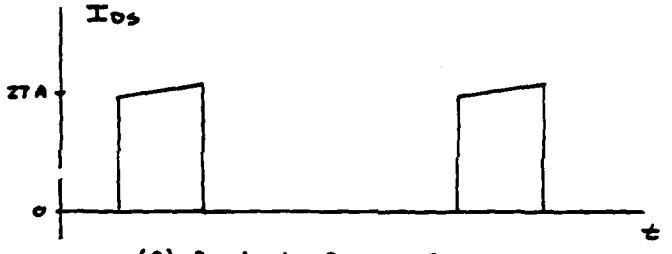
Figure 2.6.1.1.1-1 RF Amplifier Power Converter Schematic



(A) Gate-to-Source Voltage



(B) Drain-to-Source Voltage



(C) Drain-to-Source Current

Figure 2.6.1.1.1-2 MOSFET Switching Waveforms

2.6.1.1.2 Power Transformer

In order to optimize the size/efficiency tradeoff, the MOSFETS are switched at a 100 kHz rate. Since they are operating in a push-pull configuration, the effective switching frequency presented to the transformer T1 is 200 kHz. A turns ratio of 3:1 was selected to allow the power converter to operate over the full 15 V to 39 V input voltage range (i.e. DC with AC variations superimposed). Turns ratio and power handling requirements, along with applied volt-seconds led to the selection of a Ferroxcube 3C8 ferrite toroidal core (#528T500) for the power converter transformer. With an outside diameter of only 1.5 inches and thickness of only 0.5 inches, this core is consistent with the size requirements, yet core losses are limited to less than 8 watts.

The primary is wound with a braid rather than wire to reduce excessive skin-effect type heating from the 27 amp, 100 kHz switching currents that each half-primary must carry during operation. The braid also helps reduce primary leakage inductance that is caused by imperfect coupling in the transformer and leads to undesirable transients. In addition, the primary is sector-wound to further reduce leakage inductance. This is accomplished simply through the paralleling of groups of windings as is illustrated in Figure 2.6.1.1.2-1. As a result, primary leakage inductances have been kept below 100 nH, or 0.5% of the transformer magnetizing inductance. This is considerably better than the 3 to 5% typically encountered.

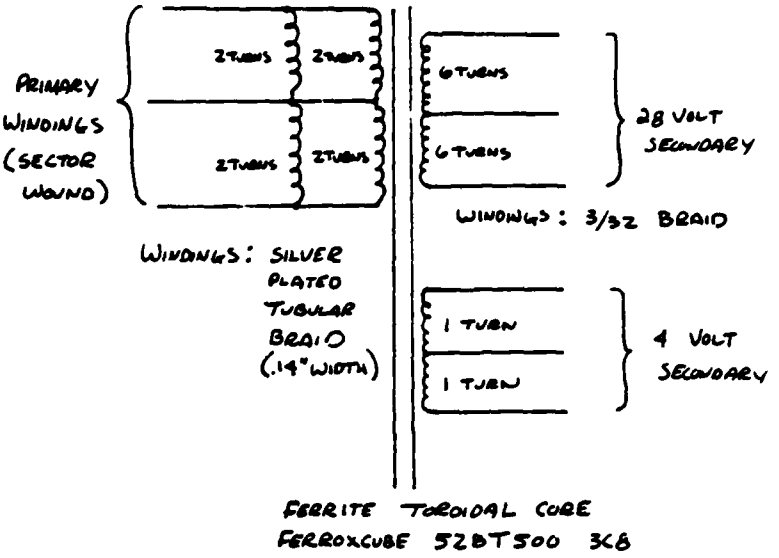


Figure 2.6.1.1.2-1 RF Amplifier Power Supply Transformer Configuration

2.6.1.1.3 Power Inductor

The coupled inductor is wound using two of the Ferroxcube toroidal cores. These differ from the transformer core only in that the inductor cores are gapped to prevent saturation. Unlike the transformer, the inductor core has a large magnetic bias applied because of the large average currents the windings must carry, and thus the need for gapping.

For proper circuit operation, the inductor turns ratio must be the same as the transformer. Both the braid and the sector type windings are used on the inductor primary to minimize leakage inductance. With the winding area nearly filled, the magnetizing inductance referred to the 28-volt secondary is greater than 100 uH, limiting the 200 kHz ripple current in the output capacitor to less than 200 mA rms. While the equivalent inductance referred to the auxiliary 4-volt winding is too small to aid in filtering the 200 kHz switching currents in this

winding, the fact that this winding stays tightly coupled to the primary output during all switching cycles (through the transformer during "on" times and through the inductor during "off" times) ensures good cross regulation between the outputs.

2.6.1.1.4 Rectifiers

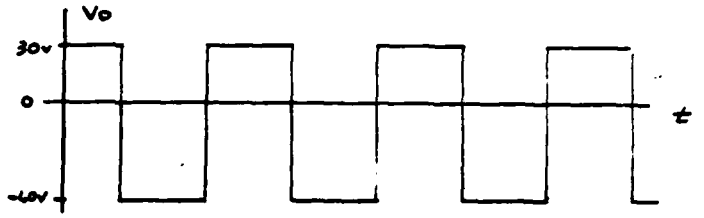
Voltage and current waveforms for the rectifier diodes associated with the 28-volt output are illustrated in Figure 2.6.1.1.4-1. 1N5814 rectifier diodes were selected for the transformer diodes because of their high current and fast switching capabilities. This in turn leads to higher power supply efficiency. The 1N5816 diode chosen for the inductor diode differs from the 1N5814 diodes only in that its peak inverse voltage rating is higher. While the transformer diodes experience reverse bias voltages of 60 volts maximum, independent of duty cycle, the reverse voltage applied to the inductor diode is as great as 90V at high line voltage. The 20 amp (at 100 degrees C) current rating of this series of diodes is ample margin for the 2.7 amps maximum the transformer diodes will carry and the 5.4 amps maximum the inductor diode will handle.

The lower current 1N5802 series of diodes is used for the auxillary output. The maximum current these diodes will carry is less than 300 mA, which is far below the 1.5 amp rating. These diodes also are fast switching diodes to minimize losses.

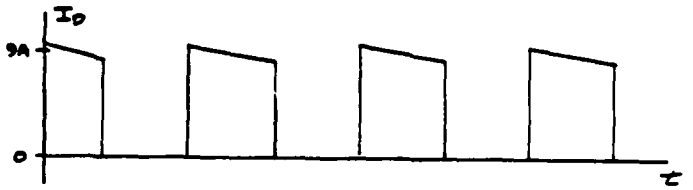
2.6.1.1.5 Output Capacitors

Output ripple voltage components below 1 MHz are required to be 20 dB below the output DC voltages. CSR-21 type tantalum capacitors were selected to provide the needed attenuation to output ripple currents. While these capacitors are ESR (equivalent series resistance) limited at 100 kHz and beyond (i.e. their impedance no longer appears capacitive above 100 kHz), they are made physically smaller than high frequency polypropylene capacitors and provide an equivalent amount of attenuation at the fundamental switching frequency where most of the ripple current energy is confined.

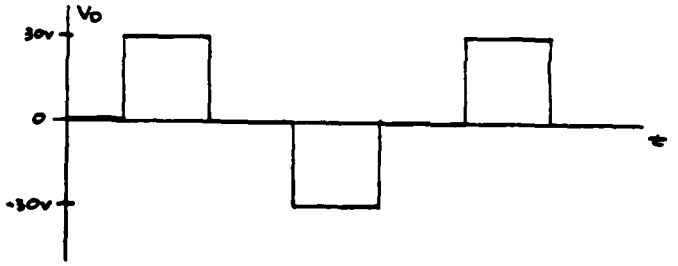
Another set of output capacitors on the primary 28-volt output, along with their series damping resistors, while not providing attenuation to output ripple currents, do aid in maintaining loop stability. Proper selection of R and C allows the loop gain to be reduced to 0 dB at the desired loop corner, while an added zero in the transfer function allows the loop phase to be brought back toward -90 degrees before loop crossover. As a result, adequate gain and phase margins over the entire range of line voltages can be maintained.



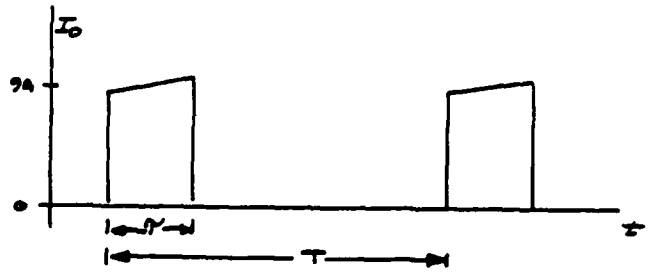
(A) Inductor Rectifier Anode Voltage Waveform



(B) Inductor Rectifier Current Waveform



(C) Transformer Rectifier Anode Waveform



(D) Transformer Rectifier Current Waveform

Figure 2.6.1.1.4-1 Rectifier Current And Voltage Waveforms

2.6.1.1.6 Snubber Networks

Even with transformer leakage inductances minimized to a fraction of a percent of the magnetizing inductance, transients that are induced can still be destructive. Snubber networks have been applied to the drains of each power MOSFET to limit voltage spikes below the 100-volt breakdown of the devices. Without the snubbers, voltages would be in excess of 300 volts.

The snubber network along with a model of the transformer are shown in Figure 2.6.1.1.6-1. With transistor Q1 turned on, the transformer primary winding carries the transformed load current (27 amps maximum). This same current passes through leakage inductance L_l and becomes the MOSFET drain-to-source current, storing energy in L_l. Note that the magnetizing inductance L_m carries only a fraction of this current -- just enough to magnetize the core. When current ceases in the MOSFET at turn-off, L_l attempts to maintain continuous current, transferring its stored energy to the capacitors through diode D_1. When the capacitor voltage reaches its peak value, the diode turns off and the capacitors are discharged through R_1 and R_2, dissipating the inductor energy as heat. This power would have otherwise been dissipated by the MOSFET.

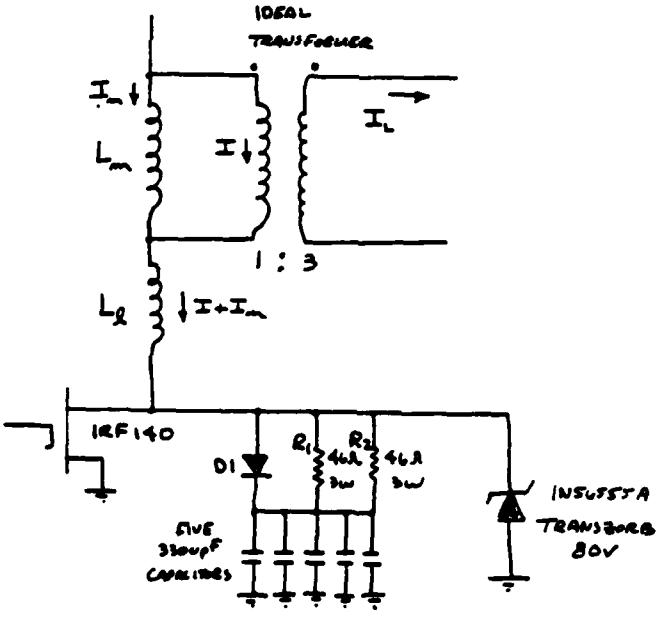


Figure 2.6.1.1.6-1 Transformer Model And MOSFET Voltage Snubbing Network

It can be shown that the peak capacitor voltage is given by:

$$V_{c\ peak} \approx V_1 + I\sqrt{\frac{L_l}{C_T}} \qquad (2.6.1.1.6\text{-}1)$$

Where V_1 = Static voltage at the transformer
I = Transformed load current
L_l = Leakage inductance
C_T = Total snubber capacitance

The power dissipated in the resistors is given by:

$$P_D = \frac{1}{2T} C_T(V_{c\ peak} - V_1)^2 = \frac{1}{2T} I^2 L_l \qquad (2.6.1.1.6\text{-}2)$$

Where T = Switching period

Thus, for a given L_l and I, the spike amplitude can be reduced to a tolerable level simply by increasing the snubbing capacitance, while power dissipation remains fixed. Note that power dissipation could be reduced, however, with a lower switching frequency. The value of resistors R_1 and R_2 are selected to ensure that the capacitor discharge time constant is much less than the minimum MOSFET "Off" time to keep charge from accumluating over a number of cycles.

The snubber capacitance consists of five ceramic capacitors so that peak currents are distributed at low enough levels to minimize heating in the capacitors. Higher current mica or plastic film capacitors would perform better here. However, the space allowed warrants the use of ceramic capacitors. The snubber resistors dissipate power during transistor "on" times as well as "off" times. The total dissipation can be as high as 3 watts, thus requiring that power resistors be used. Note the presence of the Transzorb in Figure 2.6.1.1.6-1 from drain to source. This is an 80-volt device and is only used to protect the MOSFETS from abnormal transients that might be induced elsewhere in the system. The value of snubber capacitance is chosen to keep worst case power-supply-induced spikes below the 80-volt breakdown of these devices, keeping them off during normal operation. This is necessary because these devices are only rated at 1/2 watt and are difficult to heatsink. Simple R-C type snubbers are used to suppress voltage spikes on the rectifier diodes caused by reverse recovery characteristics. Careful selection of values for these circuits allow them to be low power circuits while still providing ample suppression to inverse voltage spikes ensuring that breakdowns will not occur.

2.6.1.1.7 Regulator Loop/Control Circuits

A schematic of the control loop and other monitoring functions is shown in Figure 2.6.1.1.7-1. Much of the circuitry is contained in a single SG1526 PWM (pulse-width modulator) IC. The functions provided in this IC include: programmable soft start, variable sawtooth oscillator, pulse width modulator, error amp for loop control, foldback current limiting, as well as a stable reference voltage source.

Controlled turn-on is provided through the soft-start circuitry. When the power supply is initially turned on, a 100 uA constant current source begins charging the external soft-start capacitor towards the reference voltage. When the capacitor voltage reaches the level called for by the control loop, normal operation proceeds. The result is that the turn-on time constant of the power supply is proportional to the soft-start capacitance chosen. A 4.7 uF capacitor forces the turn-on time to be more than 120 mSec, thus aiding to reduce peak surges during power supply turn-on.

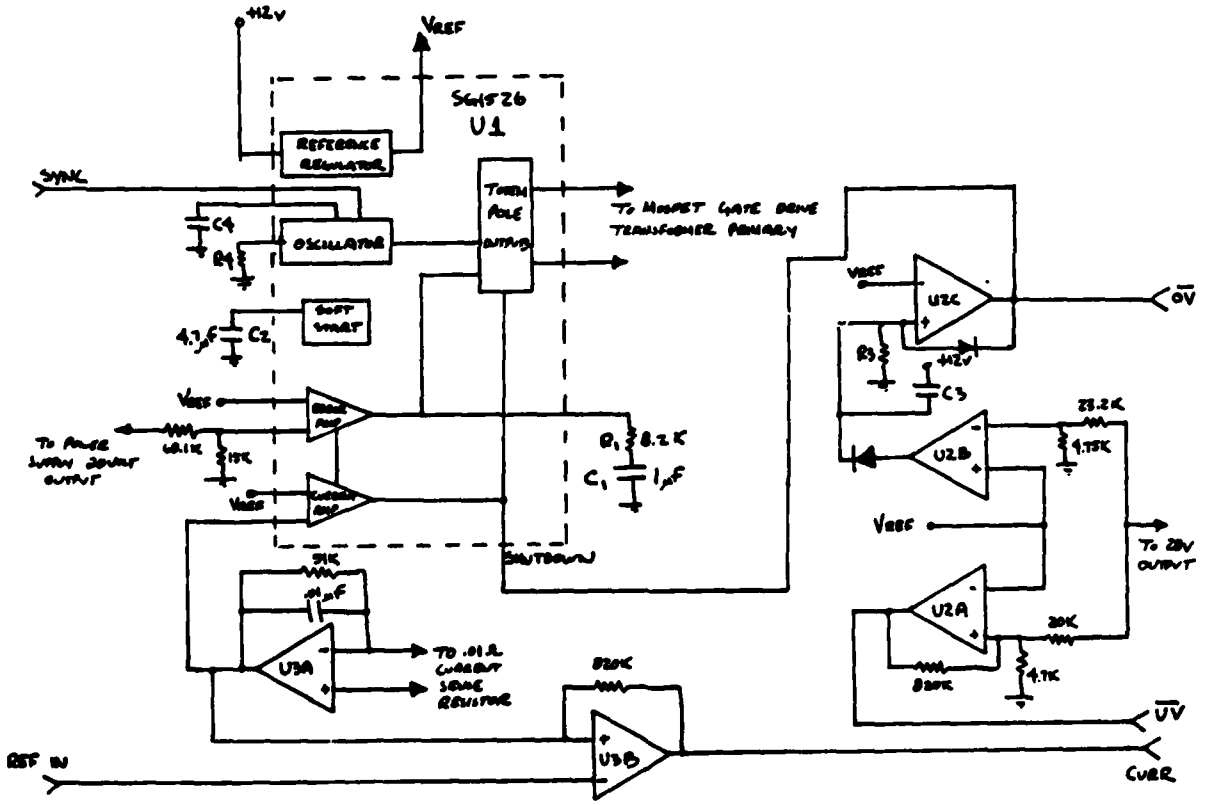


Figure 2.6.1.1.7-1 Loop Control And Monitor Function Schematic

External compensation is provided to the error amp, which has a high impedance current-source type output, so that the gain is reduced from 75 dB at DC to about 16 dB and remains flat from 20 Hz to about 1 MHz. The resulting loop gain is then high enough to provide greater than 20 dB of attenuation to line variations at low line voltages, while still low enough to maintain loop stability at highest input voltages.

Output current control is achieved through U3A. A 0.01-ohm sense resistor generates a voltage proportional to load current which is amplified by the OP-AMP and fed to the current amplifier in the PWM IC. When the 28-volt output current tries to exceed 9.8 amps, the PWM IC reduces the duty cycle linearly (and thus the output voltage drops linearly), limiting output current to 9.8 amps. The output of OP-AMP U3A is also fed to OP-AMP U3B operating as a voltage comparator. The reference to this OP-AMP is variable and provides a means by which external circuits can monitor power supply load current.

While the sawtooth oscillator fundamental frequency is adjusted to 200 kHz by components R_4 and C_4, external synchronization circuitry is also provided so that proper phasing relative to other power supplies is achieved.

Over-voltage and under-voltage functions are performed externally to the PWM IC through the use of voltage comparators U2A, B and C. One percent tolerance resistors are used to divide the output voltage down for comparison against the 5-volt reference. If the output drops below 26.6 volts, U2A signals an under-voltage condition. When the output voltage exceeds 29.5 volts, the output of U2B pulls low, causing the voltage at the input of U2C to head towards ground potential at a rate determined by the time constant formed by R_3 and C_3. If U2B continues to signal an overvoltage condition for longer than 1.5 mS, U2C signals an over-voltage condition, shutting down the PWM IC. Diodes CR_4 and CR_5 then lock U2C into a low output condition, requiring the power supply to be reset before normal operation can be resumed. The R-C time constant prevents voltage transients from shutting the power supply off, so that only static conditions are monitored.

2.6.1.2 Control Circuit Power Supply

While many similarities exist between the control circuit power supply and the RF amplifier power supply, the multiple outputs provided in the control circuit power supply lead to some problems unique to this application. Interactions between the secondary windings create difficulties in generating output filter elements that provide adequate ripple suppression characteristics while maintaining loop stabilization along with providing proper attenuation to line voltages for all outputs.

A schematic of the control circuit power supply is shown in Figure 2.6.1.2-1. Although for the most part, current and voltage waveforms that applied to the semiconductors in the RF amplifier supply also apply here, the peak values of current and voltage will be different. The peak MOSFET current, for example, is 8 amps here compared to the 27 amps in the RF Amplifier Supply, allowing the IRF 140 devices to operate with higher efficiency.

All rectifier diodes are fast recovery types, with low current devices used on the +/- 18-volt, 150-volt, and 28-volt lines, medium current diodes used on the +12-volt output, and high current diodes for the +/- 5-volt lines.

Transformer and inductor cores are the same types as used in the RF amplifier supply. Similar winding techniques are used here also. Note that the low current outputs (+28, +/-18, and 150-volts) are lacking a coupled inductor secondary. Because these outputs have light loads, if an inductor secondary had been provided it would have operated in a discontinuous current mode, acting as if it were not present.

The 150-volt output is generated through the use of another transformer tied to the 28-volt windings. The resulting waveform on the primary of this transformer is a 200 kHz rectangular wave with a 60-volt amplitude. Using the 28-volt output in this manner minimizes the needed turns ratio and wire size allowing a 0.8-inch diameter by 0.5-inch high ferrite pot core to be used to generate 150 volts, which is much smaller than would otherwise be necessary.

The regulator loop and output monitoring circuitry are nearly identical to that used in the RF amplifier supply. Resistor values, however, have been changed here to accomodate a 5-volt, 3.5-amp output (instead of a 28-volt, 9-amp output).

To meet the output ripple voltage requirements, each output must contain multiple-element output filters as shown in Figure 2.6.1.2-1. Noting that the +/- 5-volt and 12-volt outputs are fully coupled during both switching half-cycles and that the remaining outputs (i.e. those without secondary inductor windings) are coupled to all outputs during transistor "on" times, at low line voltages (maximum transistor "on" times), ripple voltages on each of the output windings are coupled to each of the remaining windings. As a worst case analysis, one must not

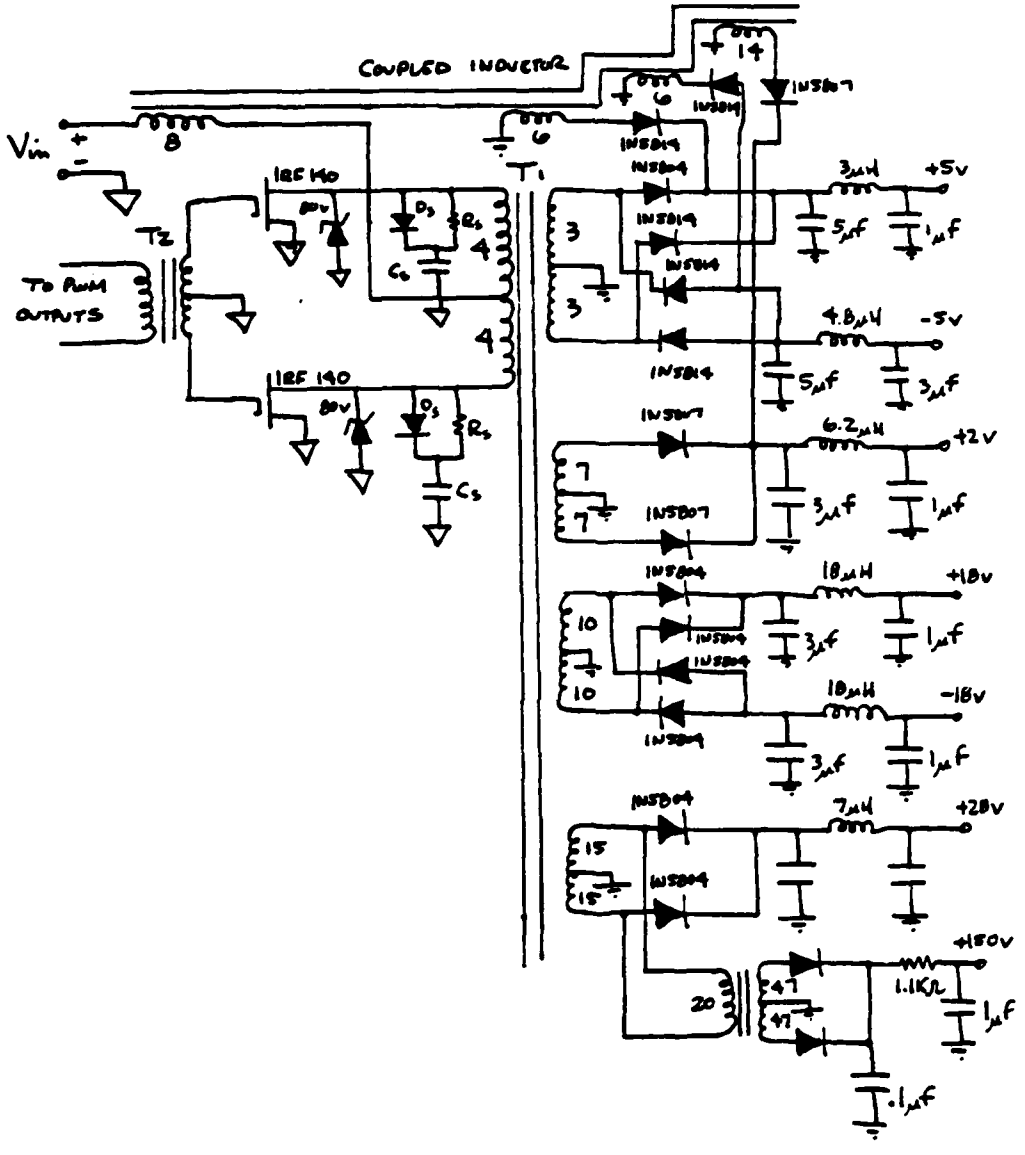


Figure 2.6.1.2-1 Control Circuit Power Supply

only include the self-induced ripple voltage for each line, but the transformed sum of all the other output ripple voltages must also be considered. As a result, the worst case ripple voltages on the cathodes (anodes for negative voltage outputs) of each winding's rectifiers will be related to any other winding's ripple voltage by the transformer turns-ratios. The L-C filter section at each output provides the remaining needing attenuation to meet ripple voltage requirements.

It is important that the output capacitors of all windings be low in value to minimize their effects on the fed-back +5-volt output. In addition, low ESR is desired in order that reasonably small values of inductance can be used between capacitors in the filter. Thus all capacitors have been chosen to be polypropylene with the exception of the damping capacitor on the fed-back +5-volt output.

2.6.1.3 Loop Considerations

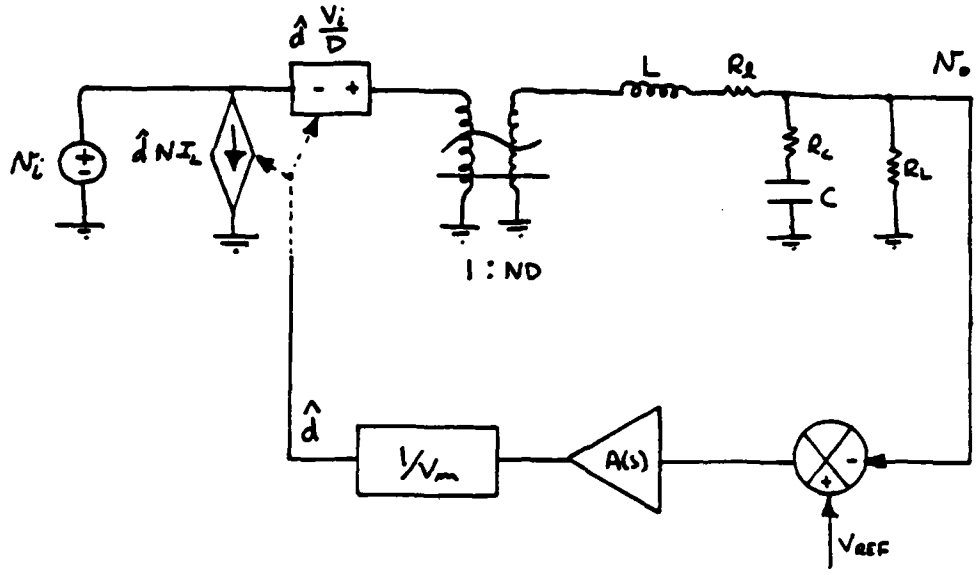
Design equations and parameters affecting the power supply control loop are presented in the following discussion.

2.6.1.3.1 RF Amplifier Power Supply

Using the state-space averaging technique as described by Middlebrock and Cuk, the small-signal model in Figure 2.6.1.3.1-1 of the RF amplifier power converter was determined. While only a brief description of the model will be provided here, a detailed derivation can be developed from the Figure.

The output filter elements include an effective load resistance R_L and output capacitor C along with its associated ESR. The effective output inductance L is equivalent to the coupled inductor magnetizing inductance as referred to the 28-volt secondary winding. A series resistance R_ℓ is included to represent semiconductor losses. The ideal transformer in the model includes the turns-ratio of the transformer T1 in the power converter along with the effects of the steady-state duty cycle. Note that this transformer is more ideal than the conventional ideal transformer in that it has DC response proportional to its turns ratio as well as unlimited AC response. The final components in the model, the voltage-controlled-voltage and -current sources at the input are a result of the AC perturbations of duty cycle and provide a means for feedback in the model.

Also included in Figure 2.6.1.3.1-1 is a model of the feedback loop which includes an error amplifier with transfer function A(s) along with the gain of the pulse width modulator. The gain can be shown to be $1/V_m$ where V_m is the peak amplitude of the sawtooth waveform in the PWM IC ($\approx$3 volts).



N_i = INPUT VOLTAGE = $V_i + \hat{N}_i$

D = STEADY STATE DUTY CYCLE

N = TRANSFORMER TURNS RATIO

$\hat{d}$ = AC DUTY CYCLE

I_L = LOAD CURRENT = $\frac{V_o}{R_L}$

N_o = $V_o + \hat{N}_o$ = OUTPUT VOLTAGE

Figure 2.6.1.3.1-1 RF Amplifier Power Supply Small-Signal Model

Expressions for a number of parameters can be derived using this model including input and output impedances along with loop response. Key expressions describing the control loop are presented below.

$$\text{Loop Gain} = T(s) = \frac{A(s)}{V_m} ND \frac{V_i}{D} H_e(s) \qquad (2.6.1.3.1\text{-}1)$$

Where
- N = Transformer turns ratio
- D = Steady state duty cycle
- $H_e(s)$ = Equivalent output filter response
- V_i = DC line voltage

$$\text{Input Impedance} = Zi(s) = \frac{1}{\frac{-T(s)}{1+T(s)}\,\frac{1}{\frac{R_L}{(ND)^2}} + \frac{1}{1+T(s)}\,\frac{1}{\frac{Z_{ei}}{(ND)^2}}} \qquad (2.6.1.3.1\text{-}2)$$

Where Z_{ei} = Output filter input impedance
$= R_L \| Z_C + Z_L$

$$\text{Output Impedance} = Z_o(s) = \frac{Z_{eo}}{1+T(s)} \qquad (2.6.1.3.1\text{-}3)$$

Where Z_{eo} = Open-loop Output Impedance
$= Z_L \| Z_C$

Audio susceptibility, which is the line-to-output transfer function, is given by:

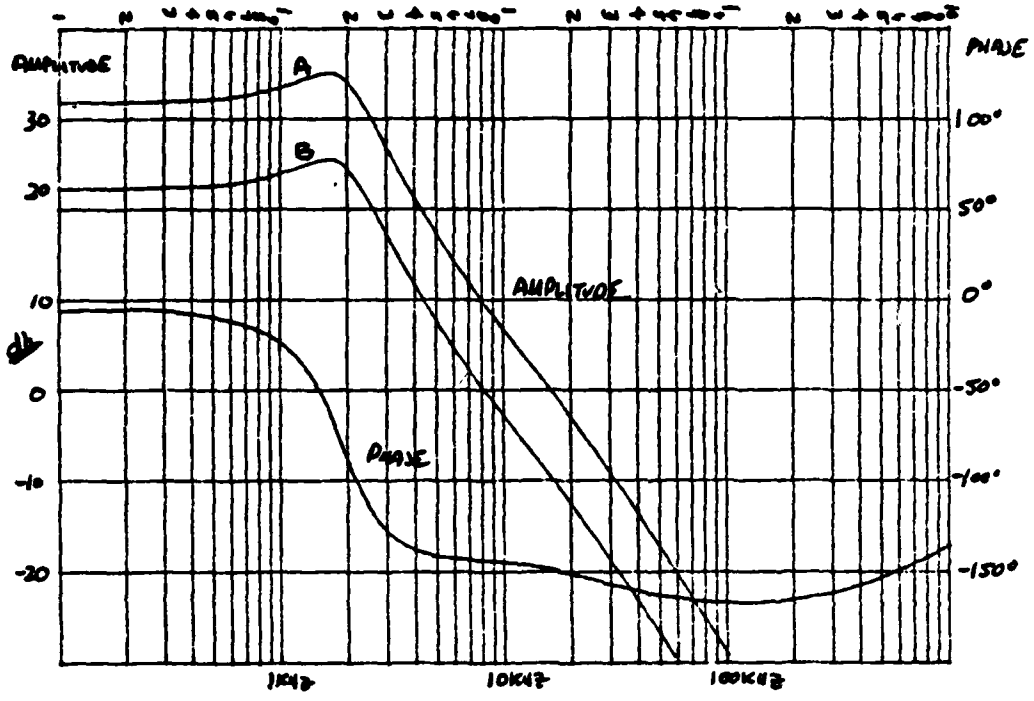
$$\frac{\hat{v}_o}{\hat{v}_i} = \frac{NDH_e(s)}{1+T(s)} \qquad (2.6.1.3.1\text{-}4)$$

An HP9825 calculator was used to generate plots of open-loop response, audiosusceptibility, and input and output impedance, which are shown in Figures 2.6.1.3.1-2, 3, 4, and 5 respectively.

From the open-loop response it can be seen that ample gain and phase margins are maintained over the entire range of input voltages. As a result, better than 20 dB of rejection to line variations is maintained in the audiosusceptibility response with little peaking incurred.

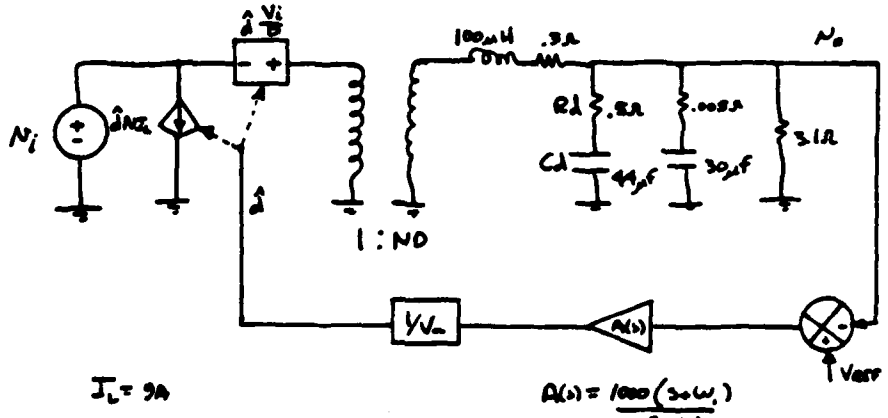
The low output impedance of the power supply ensures good transient response. However, the negative resistance exhibited by the input impedance at low frequencies will make the EMI filter design difficult as is shown in Section 2.6.2.

The effect of the damping section of the power supply output filter on the open-loop response is illustrated in Figure 2.6.1.3.1-6. Note that the output filter corner is reduced with the addition of the damping section, allowing the loop corner to be moved back in frequency. The phase also begins rolling off at a correspondingly lower frequency. However, the slope is reduced, and in fact, the phase begins coming back toward -90 degrees just before crossover. An investigation of the filter response reveals the reasons for this.



A: V_{IN} = 39v

B: V_{IN} = 13v



I_L = 9A

D = .7 V_i = 13v

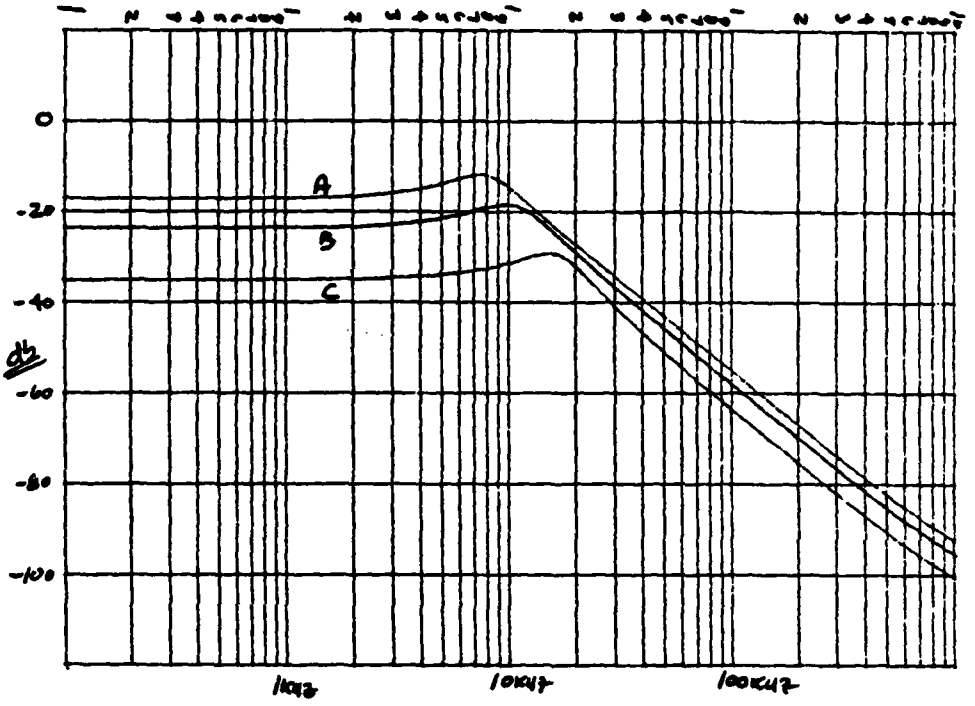
= .36 V_i = 39v

$A(s) = \frac{1000(s+\omega_1)}{s+\omega_2}$

$\frac{\omega_1}{2\pi}$ = 8.9 Hz

$\frac{\omega_2}{2\pi}$ = .01 Hz

Figure 2.6.1.3.1-2 Converter Open-Loop Response



A: V_i = 13v

B: V_i = 20v

C : V_i = 39v

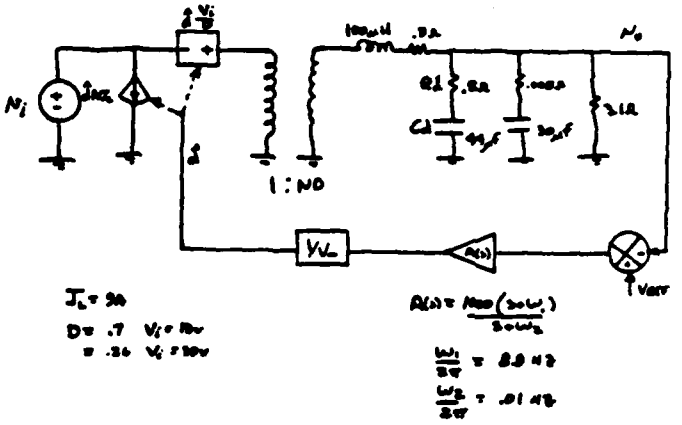
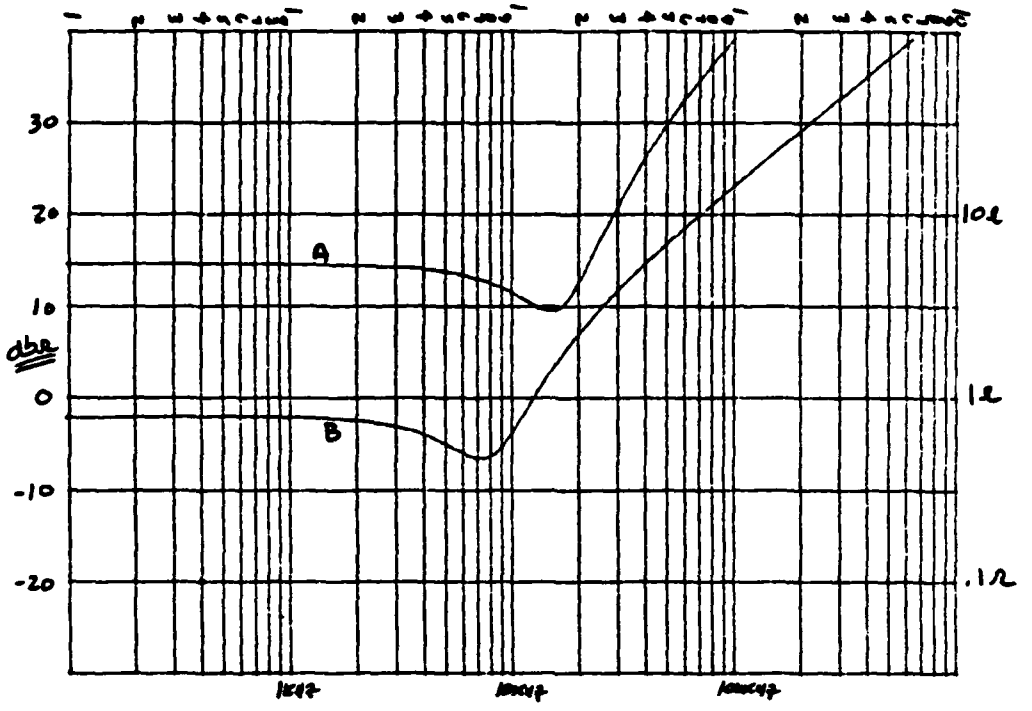


Figure 2.6.1.3.1-3 Audiosusceptability



A: V_i = 15v

B: V_i = 39v

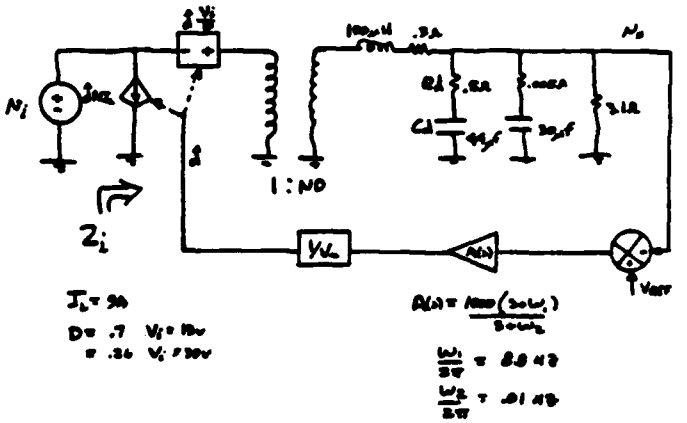
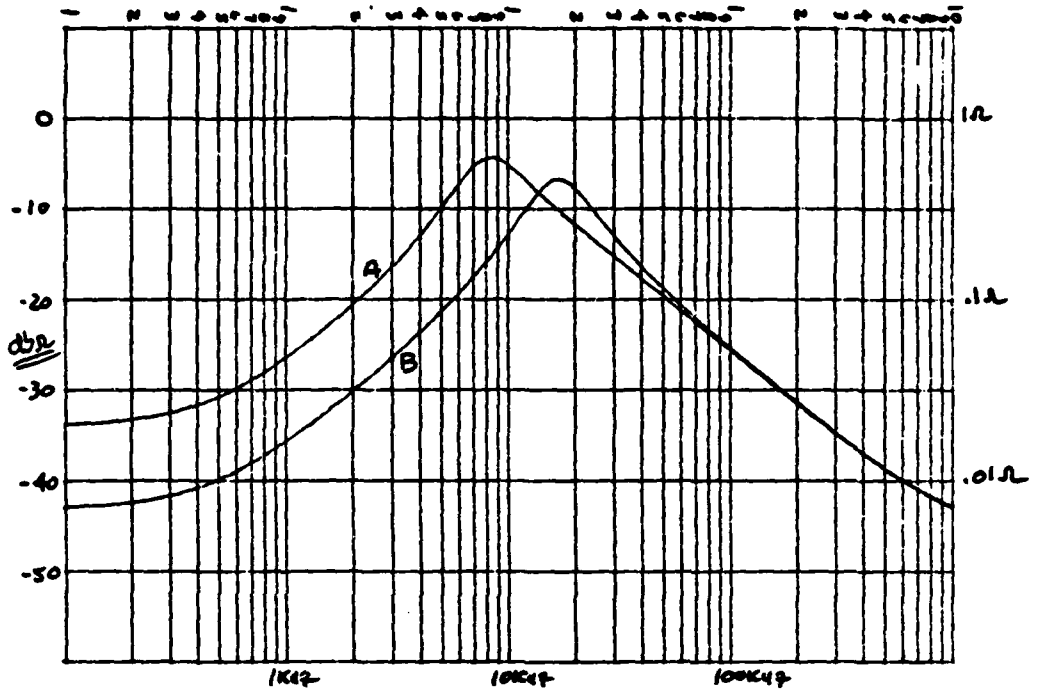


Figure 2.6.1.3.1-4 Converter Input Impedance



A: V_i = 13v

B: V_i = 39v

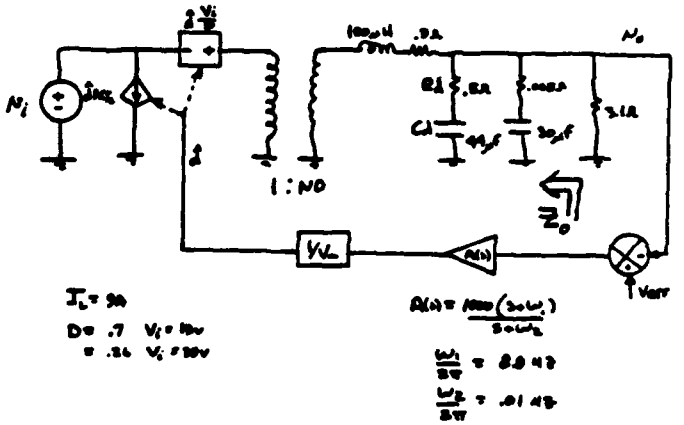
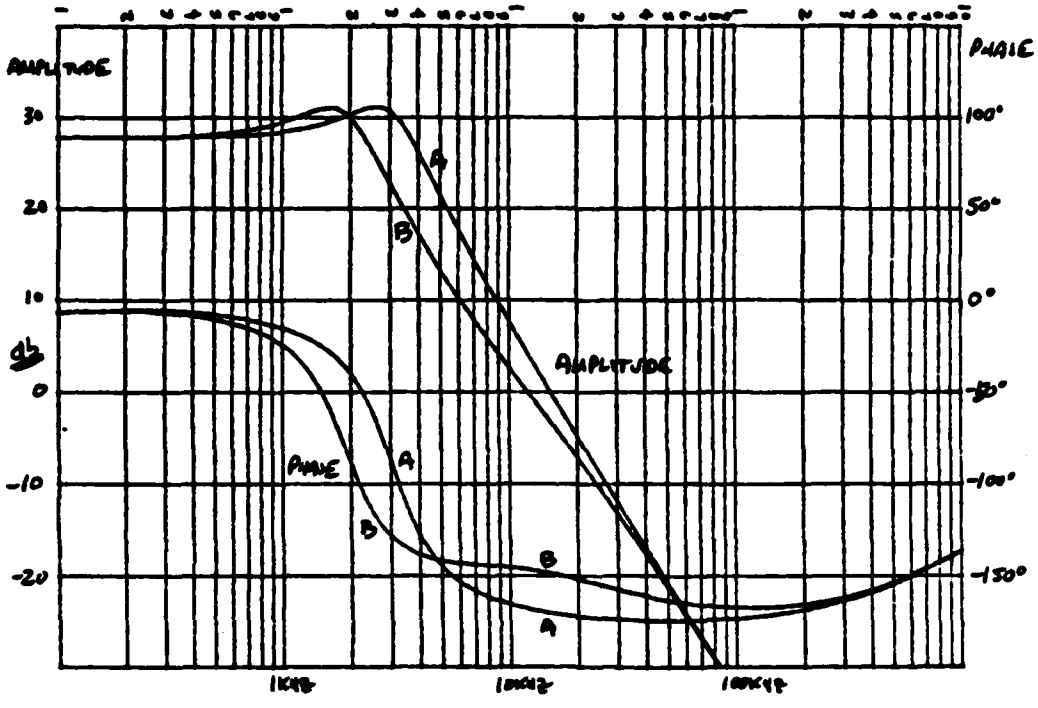


Figure 2.6.1.3.1-5 Converter Output Impedance



A: UNDAMPED OUTPUT FILTER

B: R-C DAMPING NETWORK ADDED

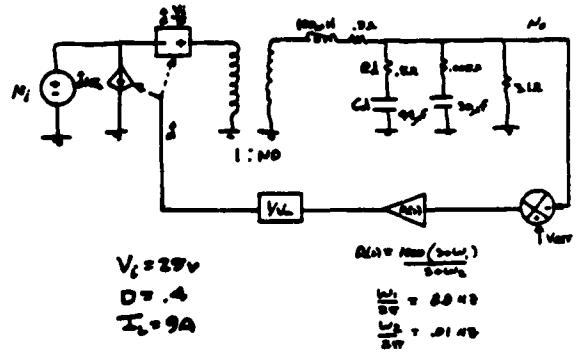


Figure 2.6.1.3.1-6 Effects Of Damping Section On The Converter Open-Loop Response At Line Voltage = 25 Volts

It can be shown that the response of the converter output filter can be expressed as:

$$H_e(s) = \frac{\frac{R_\ell}{R_L + R_\ell}(sCR_C+1)}{s^2LC\frac{(R_L + R_C)}{R_L + R_\ell} + s\left(\frac{L}{R_L + R_\ell} + (R_L \| R_\ell + R_C)\right) + 1}$$

(2.6.1.3.1-5)

From this expression two critical parameters of a second order system can be expressed.

$$w_o = \frac{1}{\sqrt{LC}}\sqrt{\frac{R_L + R_\ell}{R_L + R_C}} \qquad (2.6.1.3.1\text{-}6)$$

$$2\zeta = \frac{\frac{R_o}{R_L + R_\ell} + \frac{R_L \| R_\ell + R_C}{R_o}}{\sqrt{\frac{R_L + R}{R_L + R_C}}} \qquad (2.6.1.3.1\text{-}7)$$

Where $R_o = \sqrt{L/C}$

ζ = Damping Factor

w_o = Resonant Frequency

Using these parameters the expression for filter frequency response simplifies to:

$$H_e(s) = \frac{\frac{R_L}{R_L + R}\left(\frac{s}{w_3} + 1\right)}{\left(\frac{s}{w_1} + 1\right)\left(\frac{s}{w_2} + 1\right)} \qquad (2.6.1.3.1\text{-}8)$$

Where $w_3 = 1/RC$

$$w_1 = w_o\left(\zeta + \sqrt{\zeta^2 - 1}\right)$$

$$w_2 = w_o\left(\zeta - \sqrt{\zeta^2 - 1}\right)$$

For $\zeta < 1$, the system is underdamped and the transfer function exhibits a zero and two complex poles. For $\zeta \geq 1$, the system is overdamped and the transfer function exhibits a zero and two real poles. For the case at hand without the damping section, $\zeta < 1$ and the zero occurs at high frequencies.

With the addition of the damping section, the combined impedance loci of the output capacitor in parallel with the damping section looks like that shown in Figure 2.6.1.3.1-7. At low frequencies, i.e.

$$w < \frac{1}{\frac{C_d C}{C_d + C}\,(R_d + R_C)} \qquad (2.6.1.3.1\text{-}9)$$

the combined impedance looks like a single capacitor, $C_1 = C + C_d$, and series resistance $R_C' = R_d C_d/(C_d + C)$. At high frequencies, $C' = C(R_C + R_d)/R_d$ and $R_C' = R_d \| R_C$ which reduce to $C' = C$ and $R_C' = R_C$ for the case where $R_d \gg R_C$. As a result, the damping factor of the output filter response increases around the filter corner (and loop corner), while at high frequencies the original underdamped response returns so that effective filtering of ripple voltages is maintained.

Optimally, R_d and C_d should be selected so that $\zeta = 1$ and $1/(2\pi R_d C_d)$ is equal to the loop corner frequency. This allows the amplitude response to fall off at 40 dB/decade from w_o out to the loop corner. The zero in the transfer function then does not affect the amplitude response inside the loop corner, yet begins bringing the phase back to -90 degrees one-half of a decade below the loop corner. All this leads to large gain and phase margins.

While the values chosen for the damping section in the RF amplifier power supply do not result in the ideal case of $\zeta = 1$, damping is increased and phase is reduced, but wide bandwidth is also maintained. In general, a tradeoff between bandwidth and damping will occur governed by acceptable gain and phase margins.

2.6.1.3.2 Control Circuit Power Supply

As mentioned previously, the presence of multiple outputs in the control circuit power supply leads to design difficulties. The fact that some outputs are fully coupled to the primary output and others are coupled only during transistor "on" times further complicates matters.

The state-space averaging technique was used to determine the effects of auxillary winding load impedances on the primary output. Impedances loading those outputs which contain a coupled inductor secondary are transformed directly according to the transformer turns ratios to the

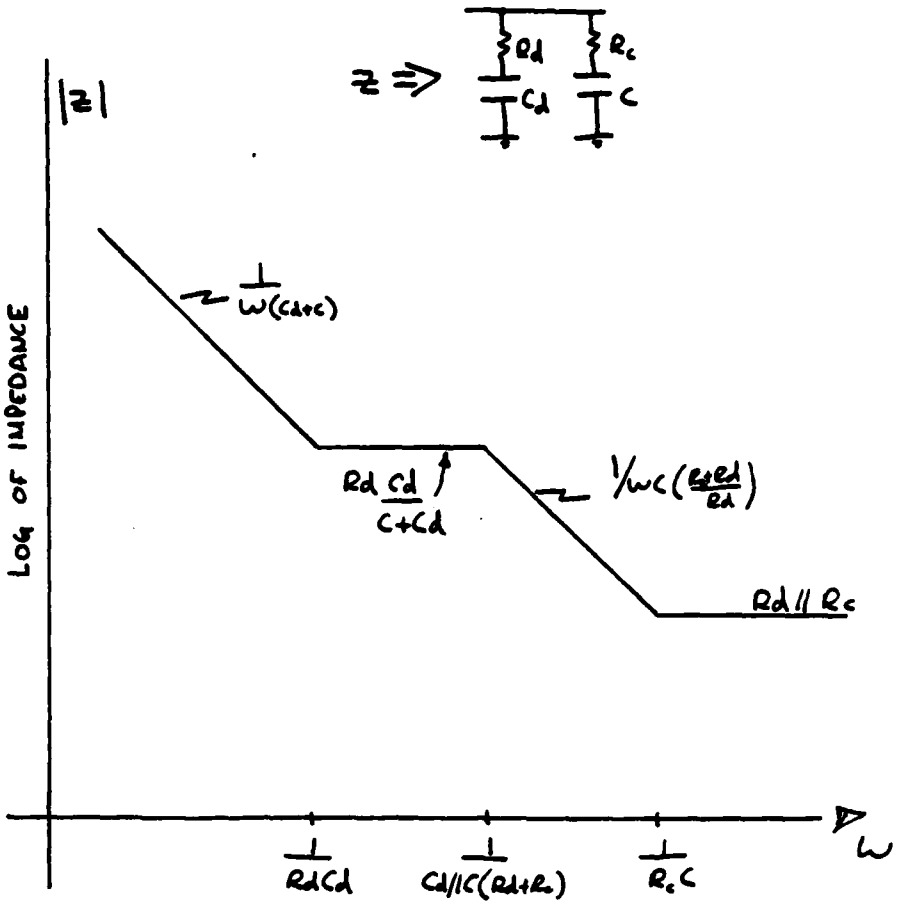


Figure 2.6.1.3.1-7 Impedance Loci Of The Parallel Combination Of Output Capacitors

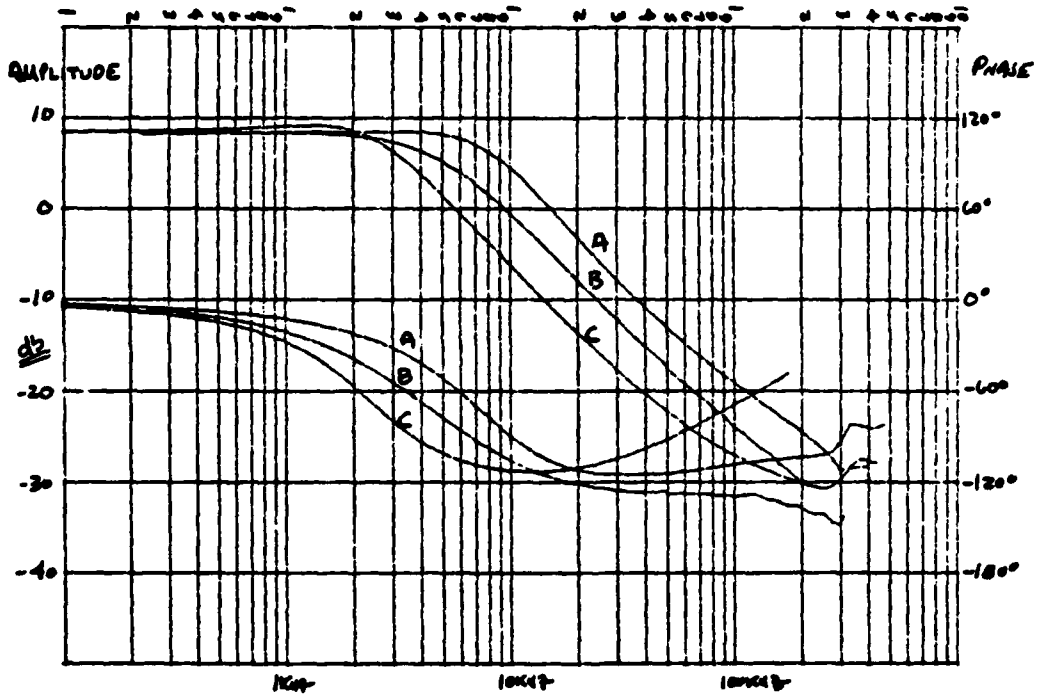
primary output, while impedances loading outputs without coupled inductor secondaries have duty cycle dependent effects. At 100 percent duty cycle, these outputs become fully coupled and the load impedances transform according to transformer turns ratios. For D = 0 these outputs become totally uncoupled and have no effect on any other outputs. For other values of duty cycle the load impedances transform according to a complex relationship. However, the two extreme cases in duty cycle also represent the extremes in effects and are adequate to consider for design purposes.

In order to verify these results, measurements on the breadboard control circuit power supply were made. The open-loop response from the error amplifier output to the primary 5-volt output was recorded under three conditions: (1) with all other outputs unloaded, (2) with only a single output with a coupled inductor secondary loaded, and (3) with only one output without a coupled inductor secondary loaded. The results are

presented in Figures 2.6.1.3.2-1, 2, and 3 for various duty cycles.

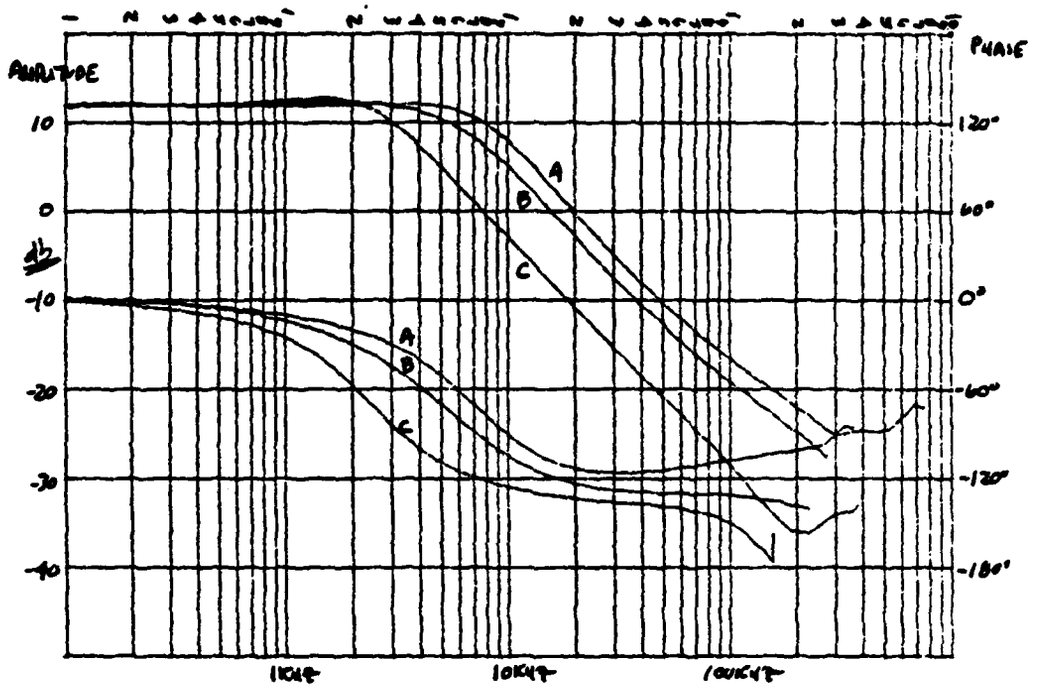
Note that load variations on the 12-volt output, which contains a coupled inductor secondary, have an equal effect on open-loop response regardless of duty cycle. Load variations on the 28-volt output (which has no inductor secondary) have a significant effect with a 15-volt input (D = 0.6), but little effect at 30 volts (D = 0.3).

It becomes clear at this point why it is important that the values of capacitors on all auxillary outputs be minimized. Not only will this help reduce variations in the loop response with duty cycle, but it will enable a reasonable damping network to be implemented on the primary 5-volt output that will not be swamped-out by impedances transformed from other windings.



A: +5V LINE LOADED ONLY
B: +28V LINE & 5V LINE LOADED
C: +12V LINE & 5V LINE LOADED
V_i = 15 VOLTS, D = .6

Figure 2.6.1.3.2-1 Measured Response In Control Circuit Supply For D = 0.6



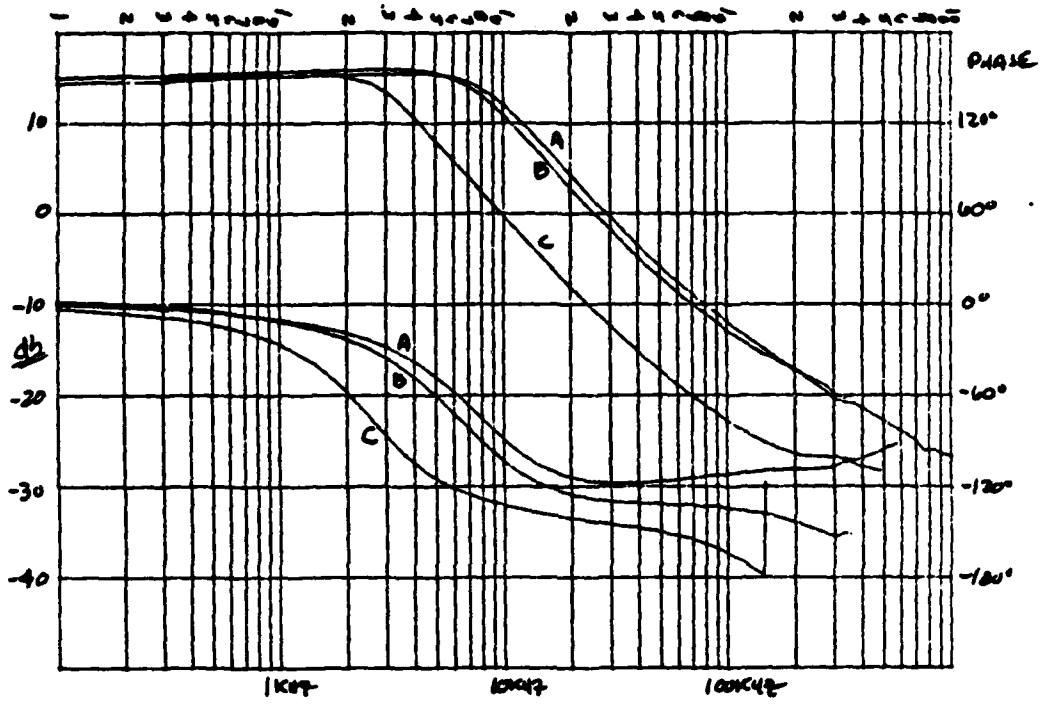
A: 5v LINE ONLY LOADED

B: 28v LINE & 5v LINE LOADED

C: 12v LINE & 5v LINE LOADED

V_i = 20v , D = .42

Figure 2.6.1.3.2-2 Measured Response For D = 0.4



A: 5V LINE LOADED ONLY

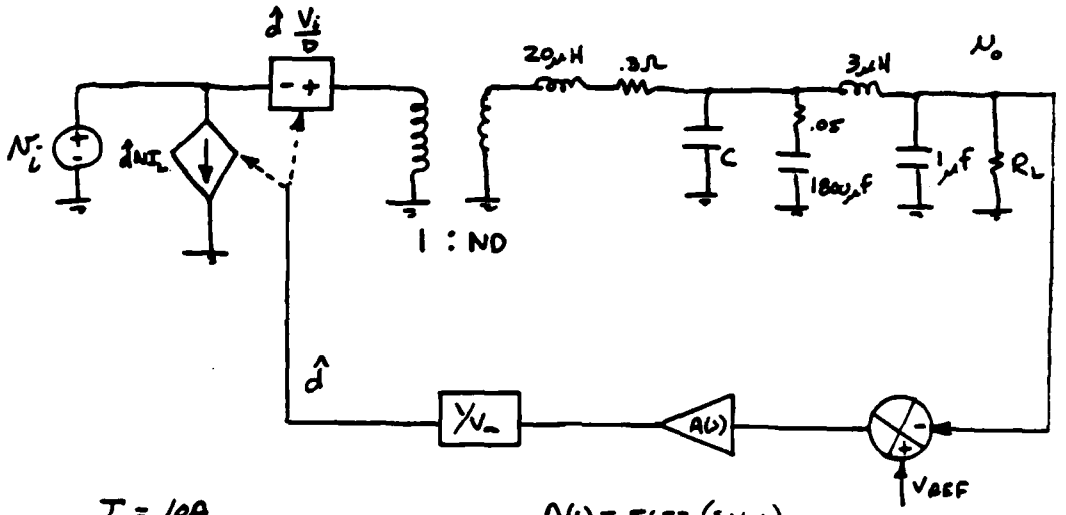
B: 28V AND 5V LINES LOADED

C: 12V AND 5V LINES LOADED

$V_i = 30V$, $D = .3$

Figure 2.6.1.3.2-3 Measured Response For D = 0.3

The resulting small-signal model of the control circuit power supply is shown in Figure 2.6.1.3.2-4 with loop response, audio susceptibility, and output impedance plotted in Figures 2.6.1.3.2-5, 6, and 7 for the primary 5-volt output.



$I_L = 10A$

$N = 3/4$

$D = .7$, $V_i = 13v$

$= .2$, $V_i = 39v$

$$A(s) = \frac{5623(s+\omega_1)}{s+\omega_2}$$

$\omega_1 = 2.8\pi$

$\omega_2 = .01\pi$

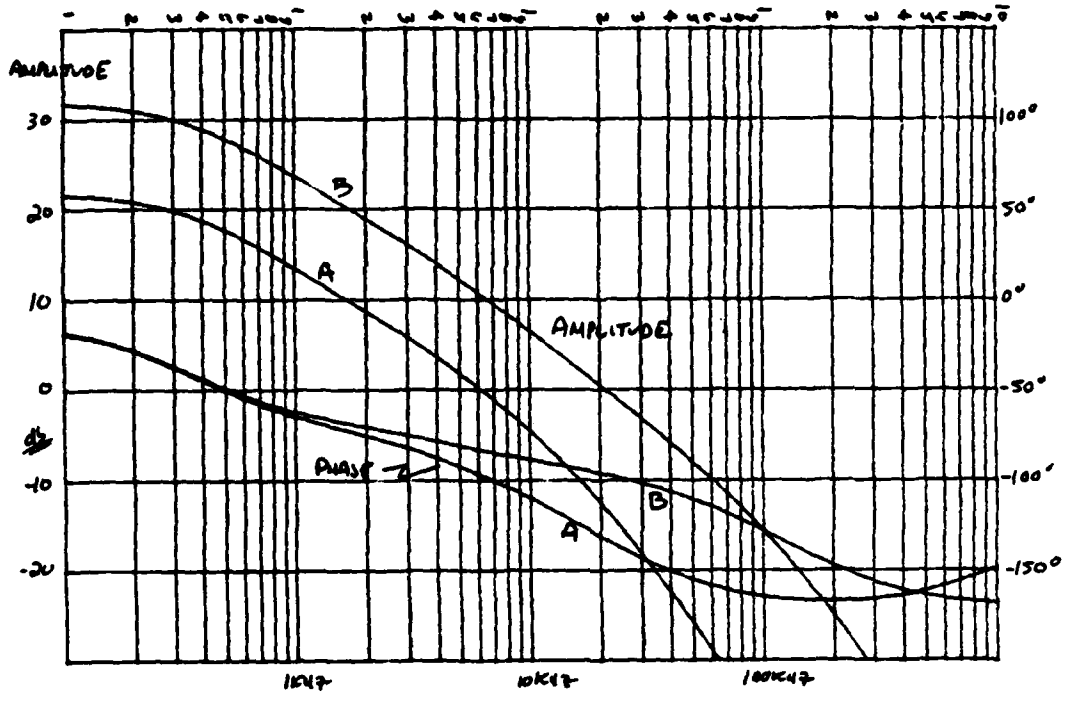
$C = 187\mu F \quad D = .7$

$= 28\mu F \quad D = .2$

$R_L = .5\Omega \quad D = .7$

$= .6\Omega \quad D = .2$

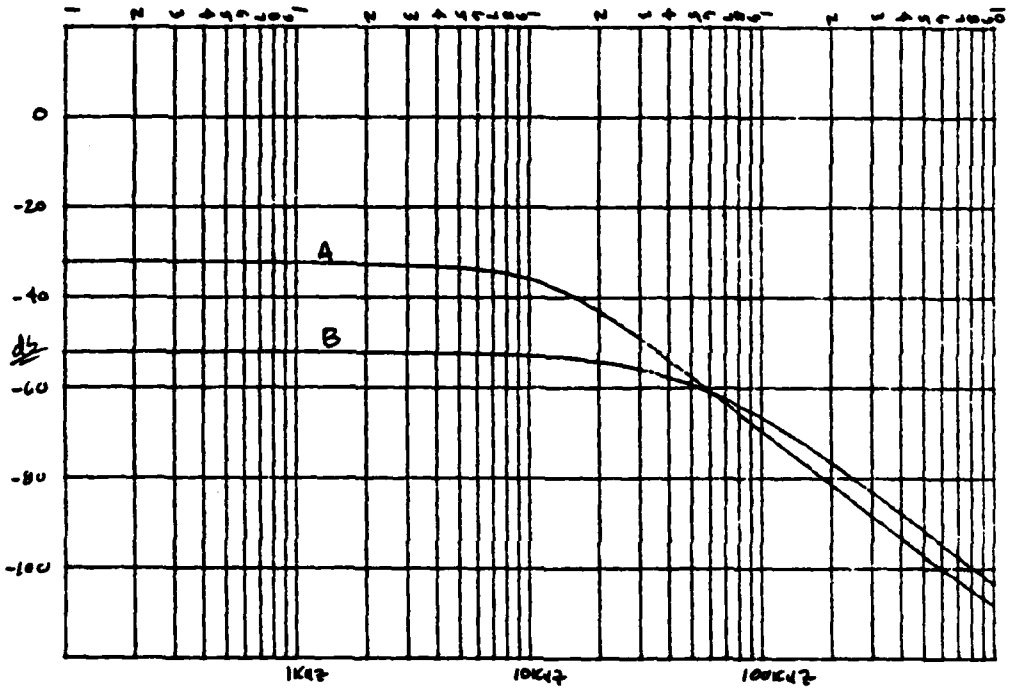
Figure 2.6.1.3.2-4 Small-Signal Model Of Control Circuit Power Supply



A: V_i = 13V

B: V_i = 39V

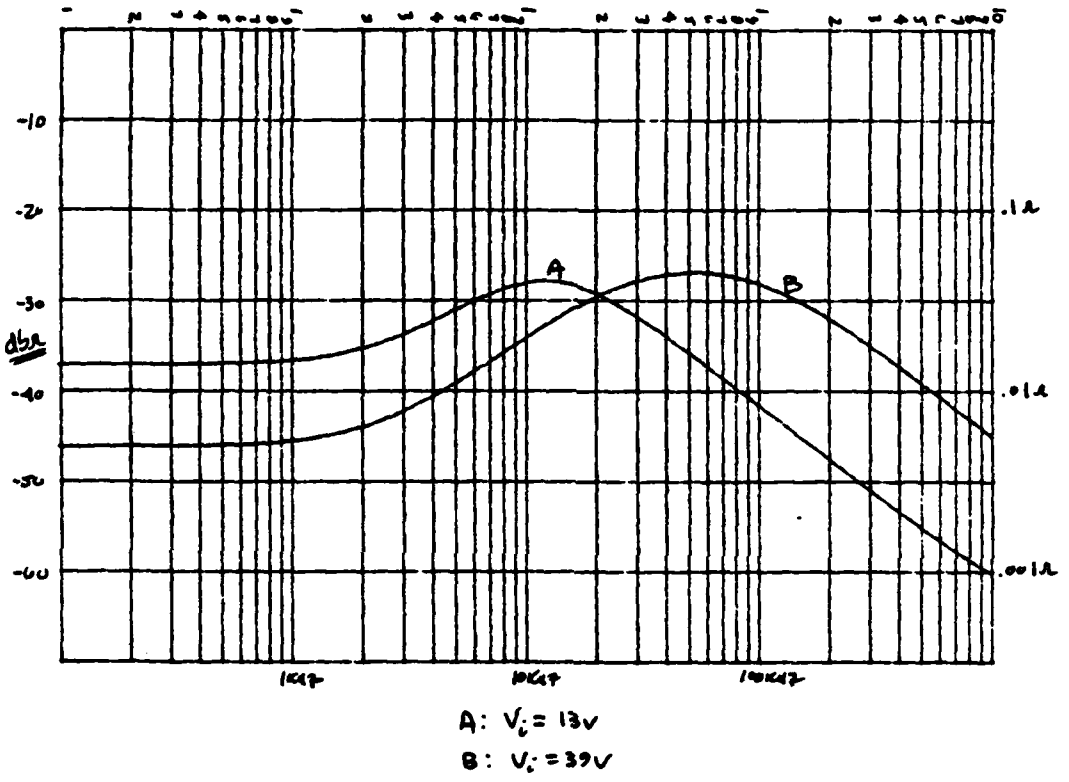
Figure 2.6.1.3.2-5 Open-Loop Response Of Control Circuit Power Supply



A: $V_i = 13V$

B: $V_i = 39V$

Figure 2.6.1.3.2-6 Audiosusceptability Response Of Control Circuit Power Supply



A: V_i = 13V

B: V_i = 39V

Figure 2.6.1.3.2-7 Control Circuit Power Supply Output Impedance

2.6.2 EMI Filter Design

The design of the input power EMI (electromagnetic interference) filter for the power amplifier is described in this section. The attenuation requirements, effect of the distributed power supply concept, and a description of the hardware are included.

2.6.2.1 Attenuation Requirements

From Figure 2.6-5, the limit for narrowband emissions on DC and interconnecting leads is 50 dBuA at 200 kHz. As a result of the 27-amp rectangular-wave switching currents inherent in the switched-mode power supplies, 109 dB of attenuation to these currents is needed at the fundamental 200 kHz rate in order to meet this requirement. Although the individual supplies will be phase-staggered, the case where all currents from each supply will add in phase must be considered a possibility and serves as the worst case condition for design purposes.

Since the current waveform to be filtered is rectangular, it will contain energy at harmonics of 200 kHz as well as at 200 kHz. These harmonics must also be filtered according to MIL-STD-461A, Notice 4 (tailored) (Figure 2.6-5). Table 2.6.2-1 lists worst case attenuation requirements for each harmonic to 1 MHz. If a filter is designed to meet the 200 kHz requirements, however, adequate attenuation to harmonics will likely be met.

Table 2.6.2.1-1 EMI Filter Attenuation Requirements

N	FREQUENCY COMPONENT (kHz)	WORST CASE AMPLITUDE (A RMS)	ATTENUATION NEEDED (dB)	CE04 (TAILORED) REQUIREMENT (dBuA)
1	200	12.15	109	51
2	400	5.8	110	42
3	600	4.0	110	36
4	800	3.0	114	32
5	1000	2.4	115	29

$$\text{RMS Amplitude} = \frac{2A \sin(N\pi D)}{\sqrt{2}\, N\pi}$$

Where A = Peak Amplitude of Rectangular Wave
N = Harmonic Number
D = Duty Cycle

Note: Attenuation needed calculated for the case where all converter signals add in-phase.

2.6.2.2 Effects Of Input Filters On Converters

Returning to the small-signal model of the coupled inductor push-pull converter and including an input filter with transfer function H(s) and output impedance Z(s), the effects of input filters on converter loop gain and output impedance can quickly be assessed. The loop gain with the presence of an input filter, T'(s), can be expressed as

$$T'(s) = T \frac{1 - \dfrac{Z(s)}{\dfrac{R_L}{(ND)^2}}}{1 + \dfrac{Z(s)}{\dfrac{Z_{ei}}{(ND)^2}}} \qquad (2.6.2.2\text{-}1)$$

Converter output impedance, Z'_o, becomes:

$$Z'_o = \frac{Z'_{eo}}{1 + T(s)} \qquad (2.6.2.2\text{-}2)$$

Where Z'_{eo} = Open-loop output impedance with an input filter

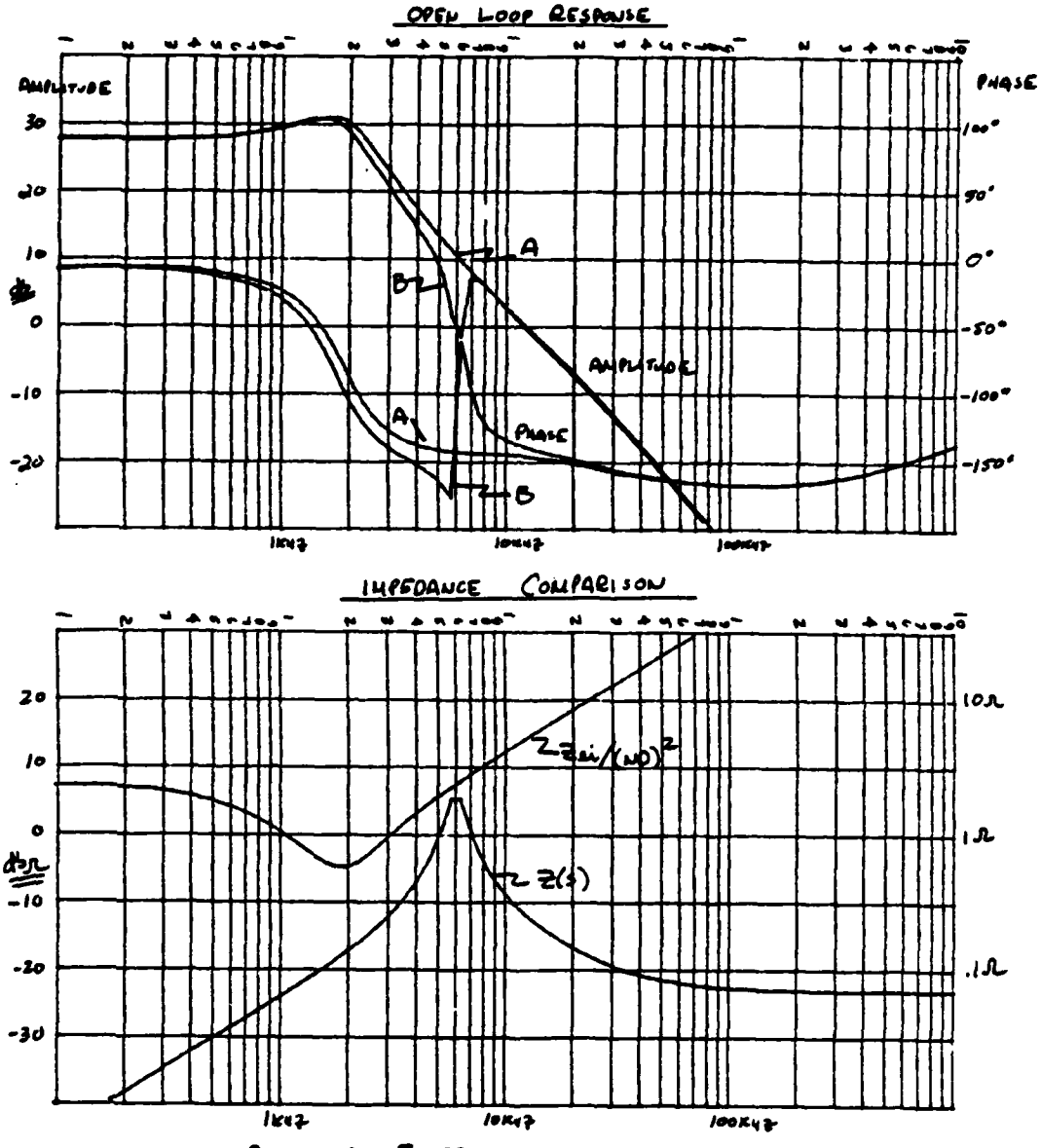
Observation of the expression for loop gain (Equation 2.6.2.2-1) reveals two inequalities which should be met in order to minimize effects of the input filter on the converter.

If $$Z(s) \ll R_L / (ND)^2 \qquad (2.6.2.2\text{-}3)$$

and $$Z(s) \ll Z_{ei} / (ND)^2 \qquad (2.6.2.2\text{-}4)$$

then $T'(s) \approx T(s)$ and both stability and good audiosusceptibility response will be assured. Note that inequality 2.6.2.2-4 includes 2.6.2.2-3 and simply requires that the output impedance of the input filter be much less than the open-loop input impedance of the switched-mode converter.

An example of what may occur if this inequality is not satisfied is presented in Figures 2.6.2.2-1 and -2. Without an input filter, the loop is stable with sufficient gain and phase margins. When an input filter is inserted with output impedance, nearly equal to the converter open-loop impedance at the filter resonant frequency, the loop becomes unstable at that point. In general, if inequality 2.6.2.2-4 is not satisfied, stability will not necessarily be jeopardized, but audiosusceptibility response and converter output impedance certainly will be affected, exhibiting large peaks where the condition 2.6.2.2-4 is not met.



A: NO INPUT FILTER

B: WITH L-C INPUT FILTER / IMPEDANCE Z(s)

Figure 2.6.2.2-1 Effects On Loop Response When $Z(s) > Z_{ei}/(ND)^2$

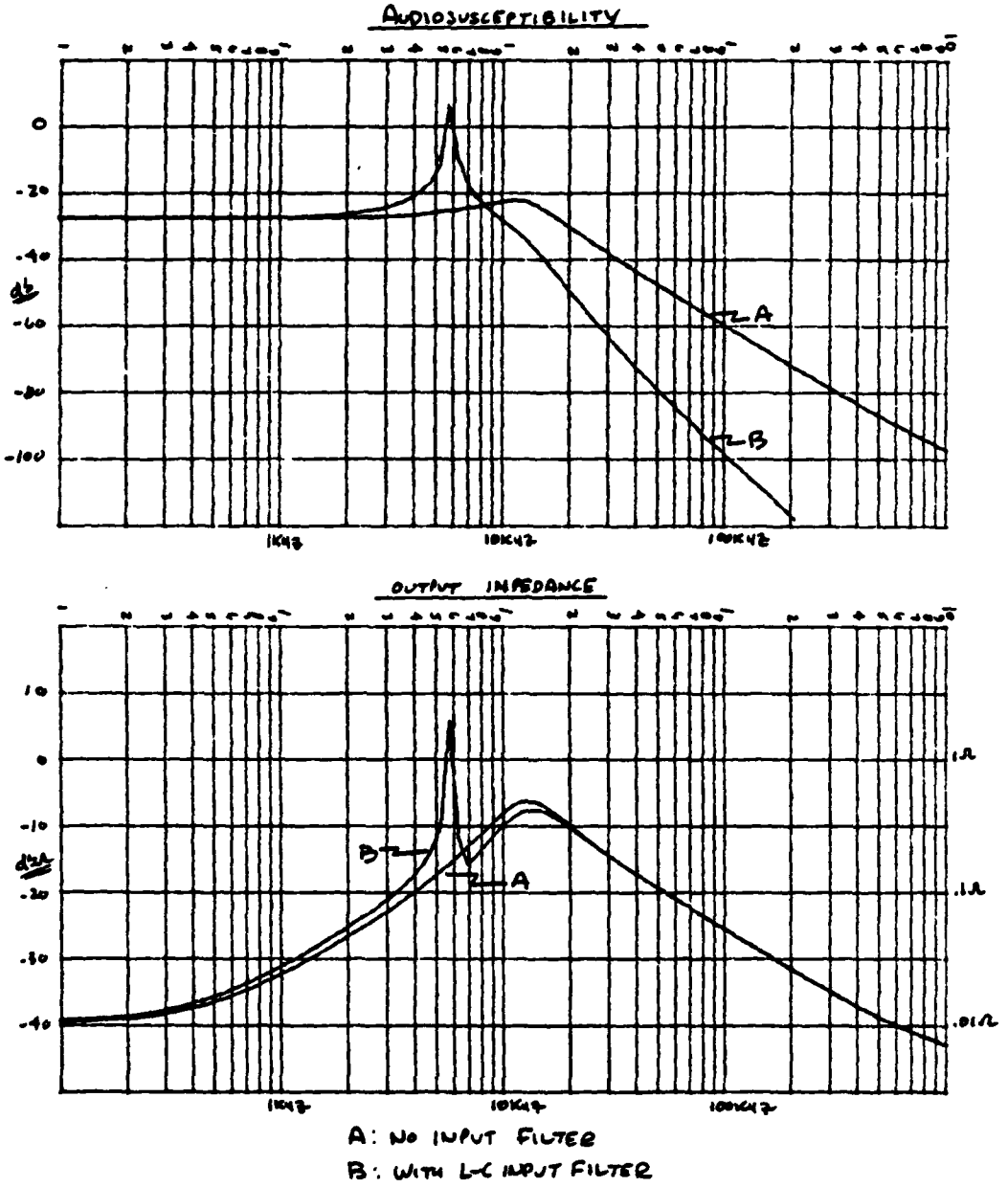


Figure 2.6.2.2-2 Effects On Audiosusceptability And Output Impedance When $Z(s) > Z_{ei}/(ND)^2$

As a result, the two major requirements for the input EMI filter are: (1) 109 dB of attenuation at 200 kHz, and (2) low output impedance -- two conflicting filter parameters. Further limits are placed on the filter when size limitations are imposed and protection against 14-volt peak-to-peak input ripple voltages from the power source must be considered.

2.6.2.3 EMI Filter Hardware Description

The final EMI filter configuration determined using the above-mentioned guidelines is shown in Figure 2.6.2.3-1. Note that in order to meet attenuation requirements, three L-C filter sections are necessary. One of the sections is built into each power converter with the driver amplifier power supply and control circuit power supply sharing a section. The total calculated response to converter currents is shown in Figure 2.6.2.3-2. Polypropylene capacitor parasitics (which were included in the calculations) have little effect on the attenuation characteristics of the filter which makes them ideal choices for filter elements.

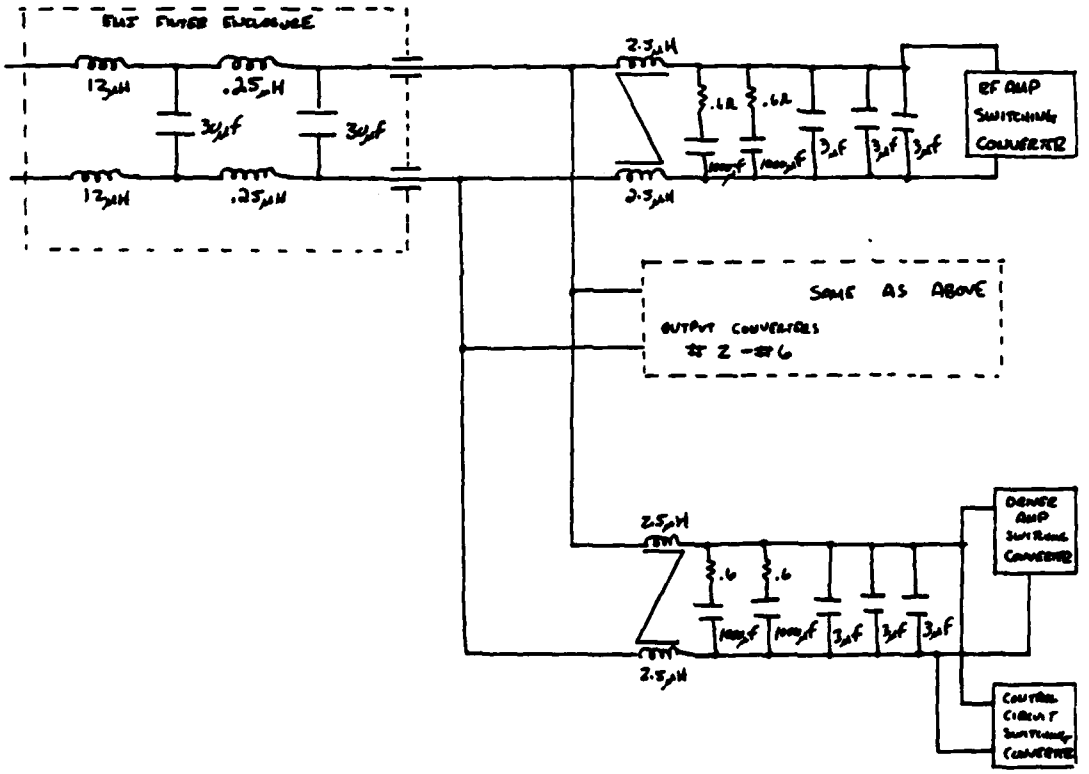


Figure 2.6.2.3-1 EMI Filter Configuration

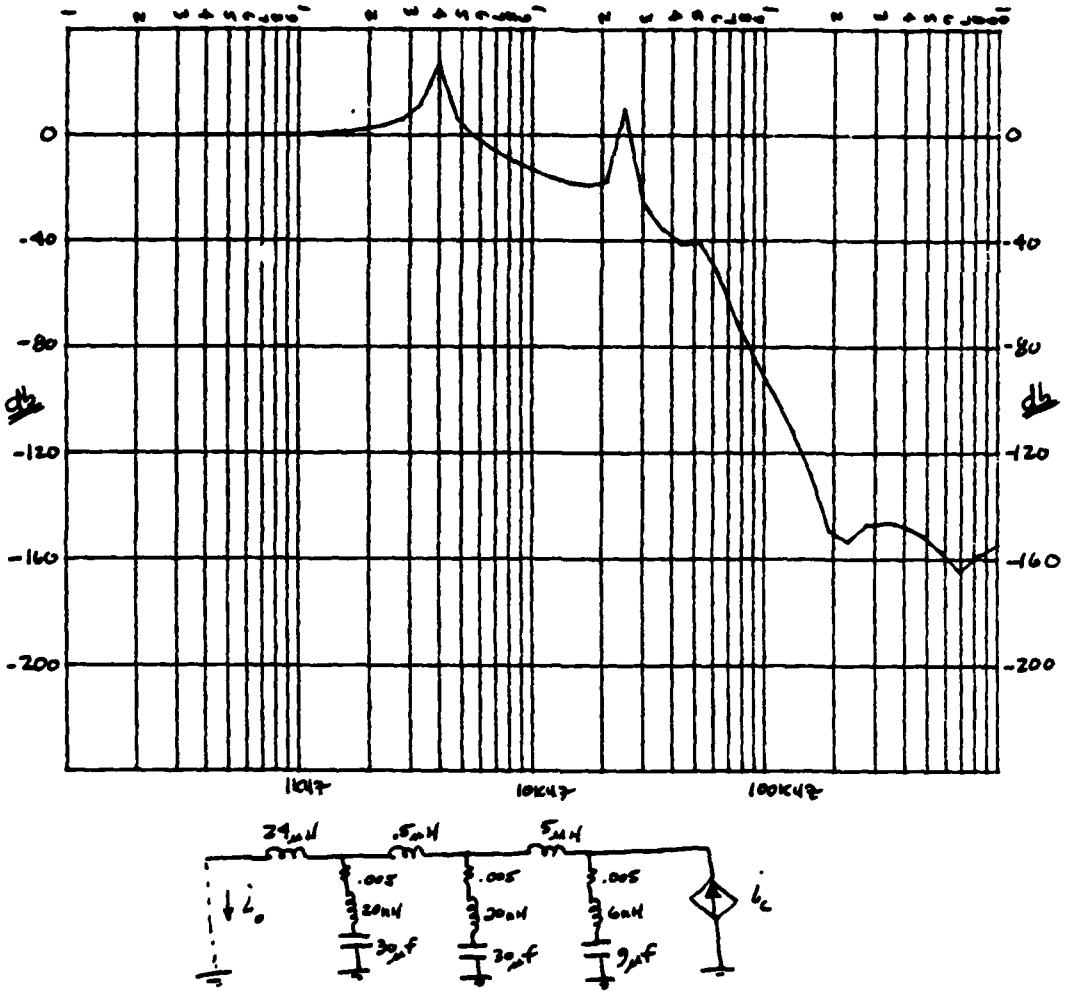


Figure 2.6.2.3-2 EMI Filter Attenuation To Converter-Induced Currents Including Capacitor Parasitics

The three 3 uF capacitors on each converter input provide the bulk of the switching currents to the converters. Each must carry 4.5 A rms in order that a switched 27 A waveform be provided to each RF amplifier converter. The 6.5 A rms rating (at 85 degrees C) of these capacitors makes them suitable choices.

The 1000 uF aluminum electrolytic capacitors along with the 1.2-ohm series resistors form damping sections on each converter input. As a result of these sections, a low impedance is presented to each converter, minimizing effects of the EMI filter on loop response. These sections are most affected by the 14 volts p-p ripple voltage that is

generated by the power source under single fault conditions. In the frequency range of 300 Hz to 3 kHz the full ripple voltage appears across the series resistors, dissipating 20 watts in each. These resistors are non-inductively wound and are imbedded in their own heatsinks, giving them a 50-watt rating. The capacitors must carry 4 A rms in this same frequency range. The Sangamo type 350 capacitors are rated at more than 5 A rms at 85 degrees C in this frequency range.

The two 2.5 uH inductors on each converter input are wound in a common-mode configuration on a single core, exhibiting more than 2.5 uH in the differential mode. Because their resulting common-mode inductance is much greater, excellent rejection of common-mode noise in either direction is obtained. The core used for this inductor is the same as those used in each power supply transformer and coupled inductor, with a gap included to prevent saturation.

A gapped laminated-iron stacked-core is used for the 12 uH inductors used in the common line to all the power supplies. The gap provided in this core is large enough to allow a 100-amp DC bias to be applied to the core while still maintaining the 12 uH inductance.

Simple air coils are used to provide the 0.25 uH inductances used in the second L-C filter section. It is important that the inductance in this section be small to minimize amplitude bouncebacks at high frequencies in the response to line voltages. Despite the low value of inductance, this section contributes nearly 30 dB of attenuation at 200 kHz.

Figures 2.6.2.3-3 through 6 show the calculated effects of the input filters along with the other six power supplies on the open-loop response of a single converter for various line voltages. In addition, a comparison of open-loop input impedance of a single converter to the total impedance presented to the converter input is provided in the Figures. Corresponding audio susceptibility responses are presented in Figure 2.6.2.3-7. Note that for this analysis all power supplies were assumed to be identical, with the driver amplifier supply and the control circuit supply combined into one equivalent RF amplifier supply.

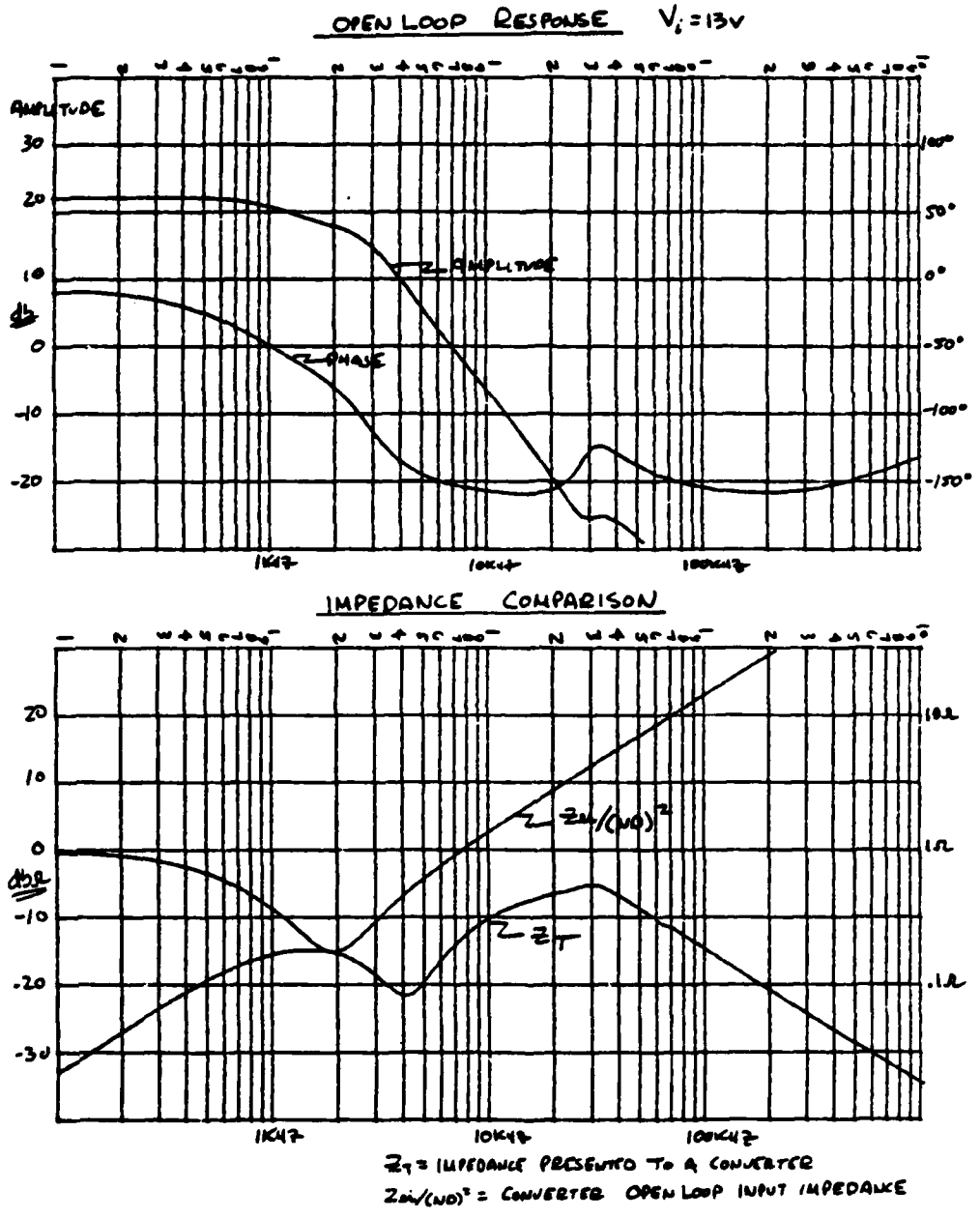


Figure 2.6.2.3-3 Converter Open-Loop Response At 13 Volts

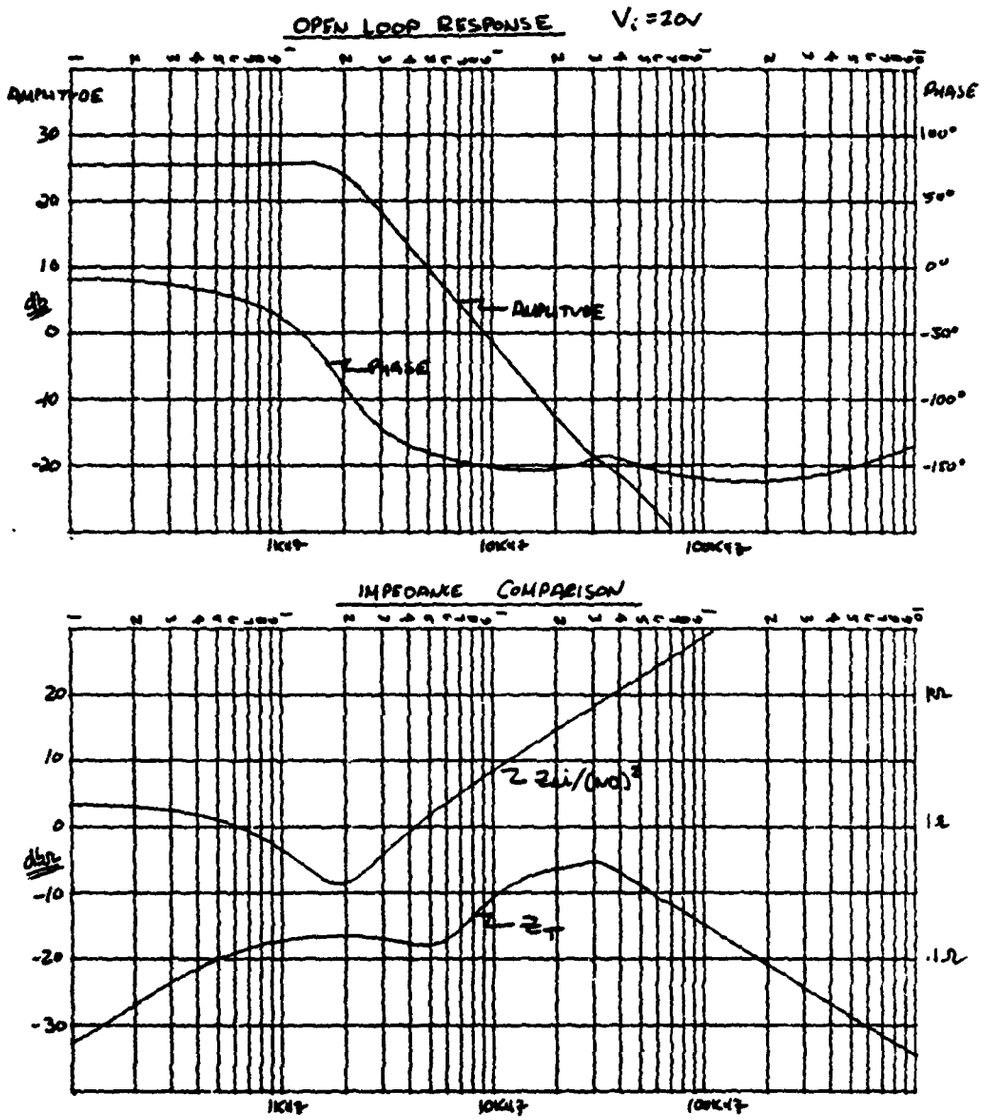


Figure 2.6.2.3-4 Converter Open-Loop Response At 20 Volts

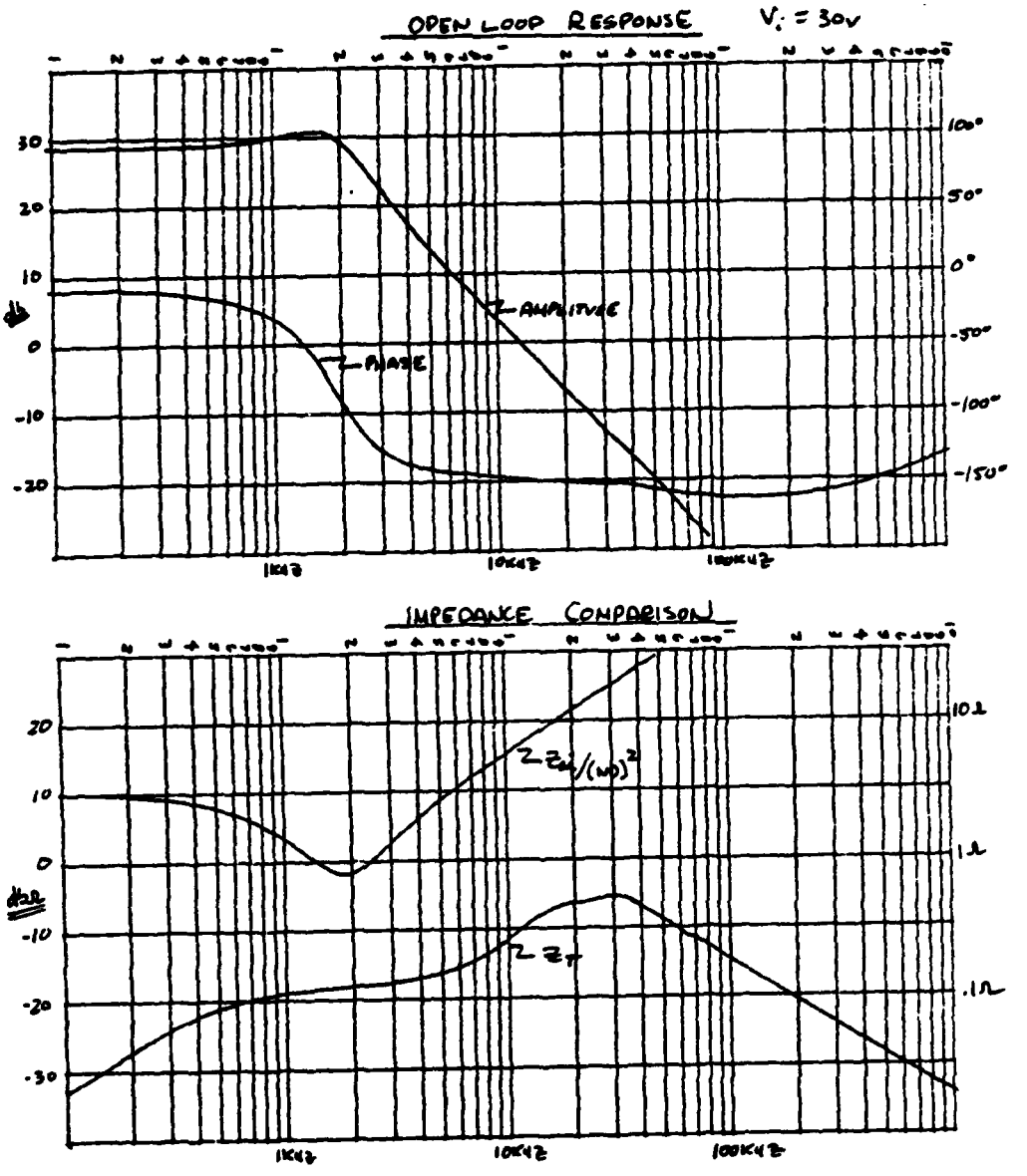


Figure 2.6.2.3-5 Converter Open-Loop Response At 30 Volts

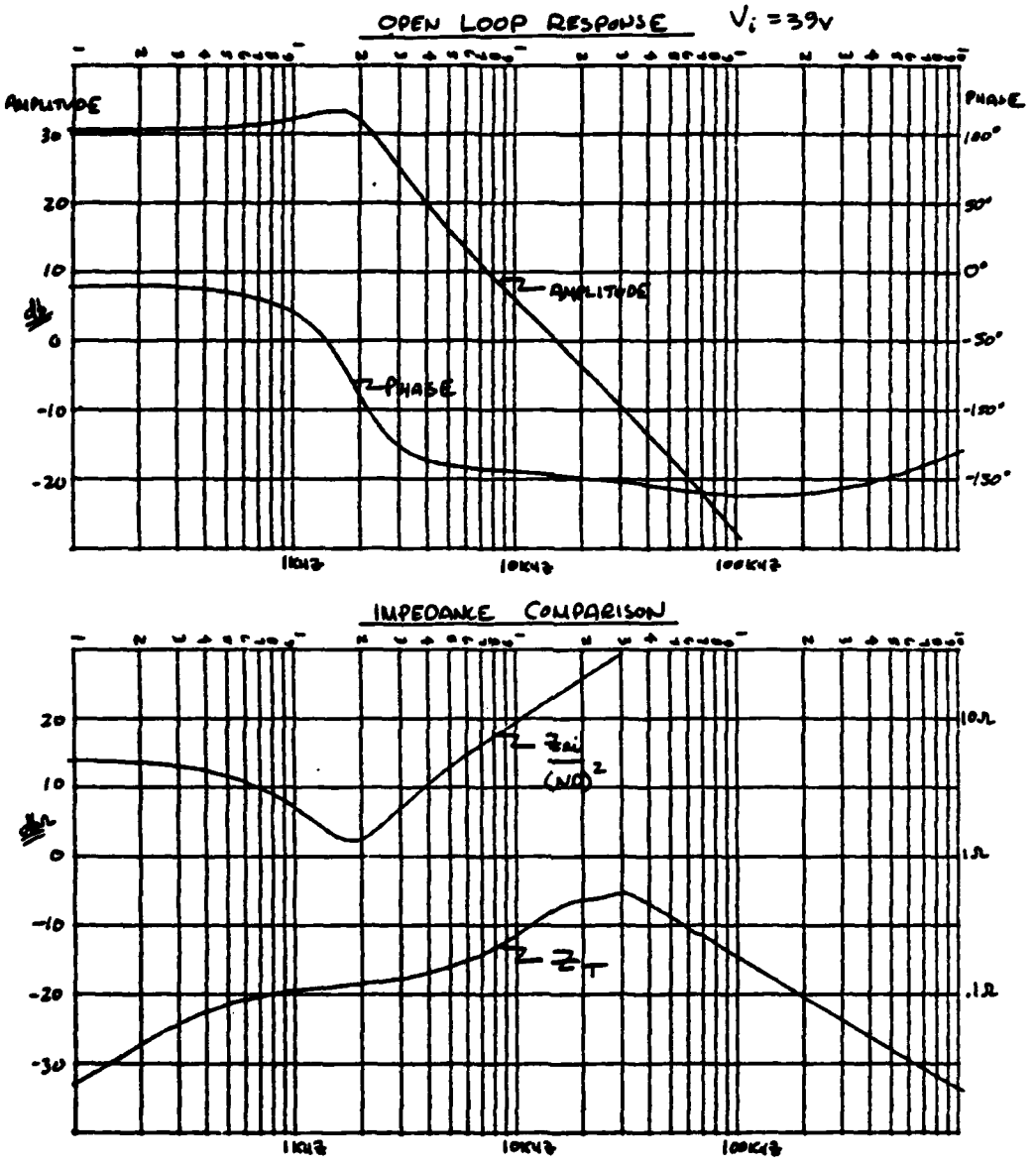


Figure 2.6.2.3-6 Converter Open-Loop Response At 39 Volts

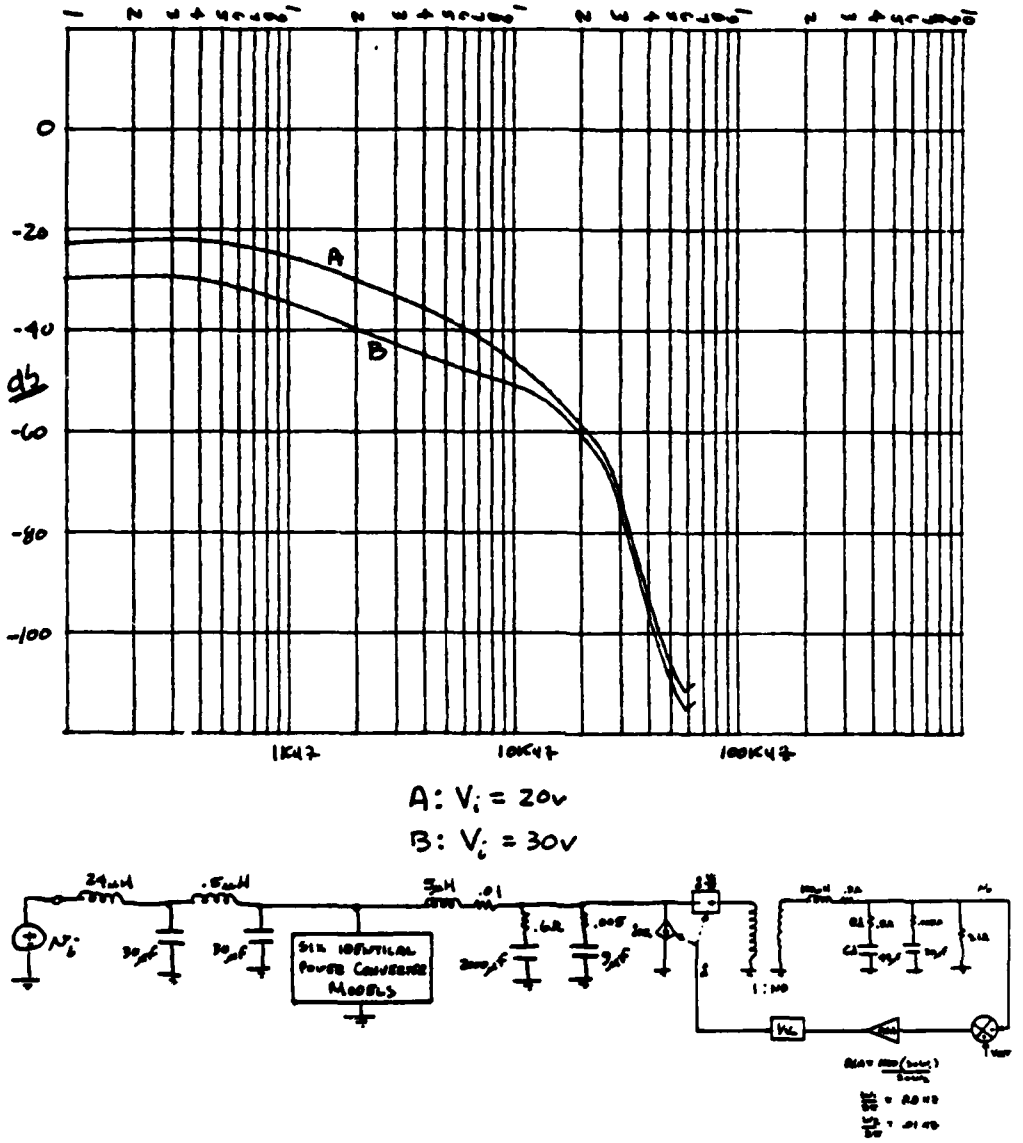


Figure 2.6.2.3-7 Converter Audiosusceptability

2.6.2.4 Effects Of Primary Power Source Impedance

In the above analysis, it was assumed that the primary power source impedance was low compared to the impedance of the EMI filter 24 uH input inductor. This is a good assumption for the case where the power source is a battery and the interconnecting cables between the battery and the power input to the power amplifier are low impedance. Under single fault conditions, however, this may not necessarily be true.

As was shown in previous sections, the input impedance of an individual power converter is negative-real at low frequencies. As a result, the total input impedance of the entire power system exhibits this negative resistance at low frequencies. (In fact, any system of switching power supplies will exhibit a negative resistance at low frequencies.) If the power source exhibits a large enough inductive impedance instabilities can occur.

Referring to Figure 2.6.2.4-1, the effect of the source impedance on an individual converter's closed-loop response A(s) is the following:

$$A'(s) = A(s) \frac{Z_i}{Z_s + Z_i} = \frac{A(s)}{1 + Z_s/Z_i} \qquad (2.6.2.4\text{-}1)$$

Assuming the converter is stable with $Z_s = 0$, in the presence of a non-zero source impedance, stability will be further assured if $1 + Z_s/Z_i$ has no roots in the right-half s-plane. For the case shown in Figure 2.6.2.4-1b where Zi = -R the low frequency input impedance of the power system and the EMI filter is modeled as the L-R-C circuit (which is accurate at low frequencies), the effective source impedance Zs becomes:

$$Z_s = \frac{(sCR_C + 1)\, sL}{s^2LC + sCR_C + 1} \qquad (2.6.2.4\text{-}2)$$

The polynomial to be evaluated for stability is:

$$1 + \frac{Z_s}{Z_i} = \frac{\frac{(sCR_C + 1)\, sL}{s^2LC + sCR + 1}}{-R} = 0 \qquad (2.6.2.4\text{-}3)$$

Rearranging:

$$s^2LC(R - R_C) + s(RCR_C - L) + R = 0 \qquad (2.6.2.4\text{-}4)$$

This equation is second order of the following form:

$$s^2A + sB + C = 0 \qquad (2.6.2.4\text{-}5)$$

with two roots given by:

$$s_{1,2} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \qquad (2.6.2.4\text{-}6)$$

For the case where A 0 or R R_C, these roots will lie in the left-half plane only if B 0. So stability will be ensured if:

$$B = RCR_C - L > 0$$

or

$$L/CR_C < R$$

Thus, a maximum total inductance L can be tolerated before the closed-loop response of a converter will contain right half plane poles. That is:

$$L < RCR_C$$

For the 500-watt power amplifier power system,

R = 0.98/7 Min = Input Negative Resistance (Ohms)
C = 7 x 1000 uF = EMI Filter Capacitance
R_C = 0.6/7 = Associated Series Resistance (Ohms)

Thus, $L_{MAX} = \frac{0.98}{7} (7 \times 2000) \frac{(0.6)}{7} = 168$ uH.

Since 24 uH of this inductance is part of the EMI filter, the total source inductance must remain below 144 uH for stability to be ensured.

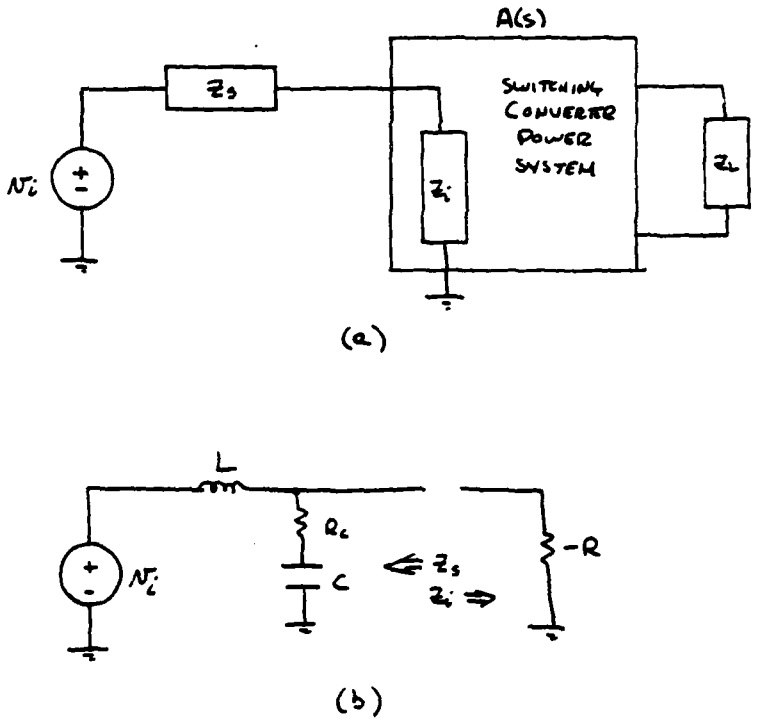
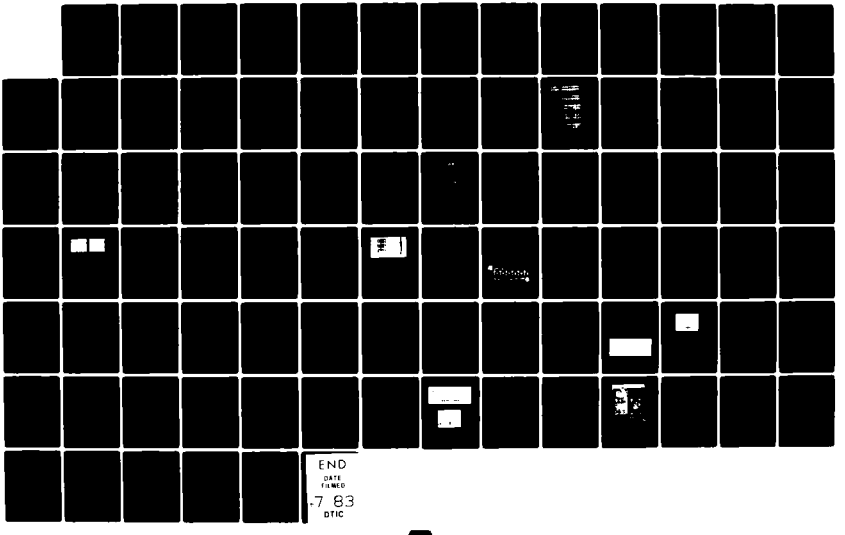
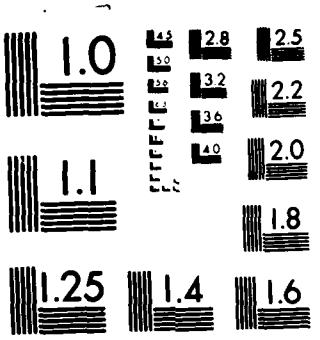


Figure 2.6.2.4-1 Modeling Of Input Source Impedance Effects

AD-A129 327 500-WATT SOLID-STATE RF POWER AMPLIFIER AM-7209( )/VRC 2/2
(U) E-SYSTEMS INC ST PETERSBURG FL ECI DIV
M BALASIS ET AL. 18 MAR 83 GO-61289-2 CECOM-82-C-J231
UNCLASSIFIED DAAB07-82-C-J231 F/G 17/2.1 NL





2.7 FILTER/DIRECTIONAL COUPLER (A6)

The low pass filter and directional coupler module contains the final RF output bandpass shaping and power control circuits for the power amplifier. Figure 2.7-1 is a block diagram of this circuit. The combined output of the six RF power amplifiers is first passed through the switched low pass filter set to remove harmonic signals generated during the amplification process. Because the frequency band is over one octave, two low pass filters are used, with the proper filter selected by the control processor based on the input frequency counter output. An RF directional coupler follows the filter assembly to sample the output forward and reflected power components. The sampled power signals are detected, and a high gain power control loop and power reference generator in this module create the feedback control signal to the variable attenuator in the driver amplifier to control the output power level.

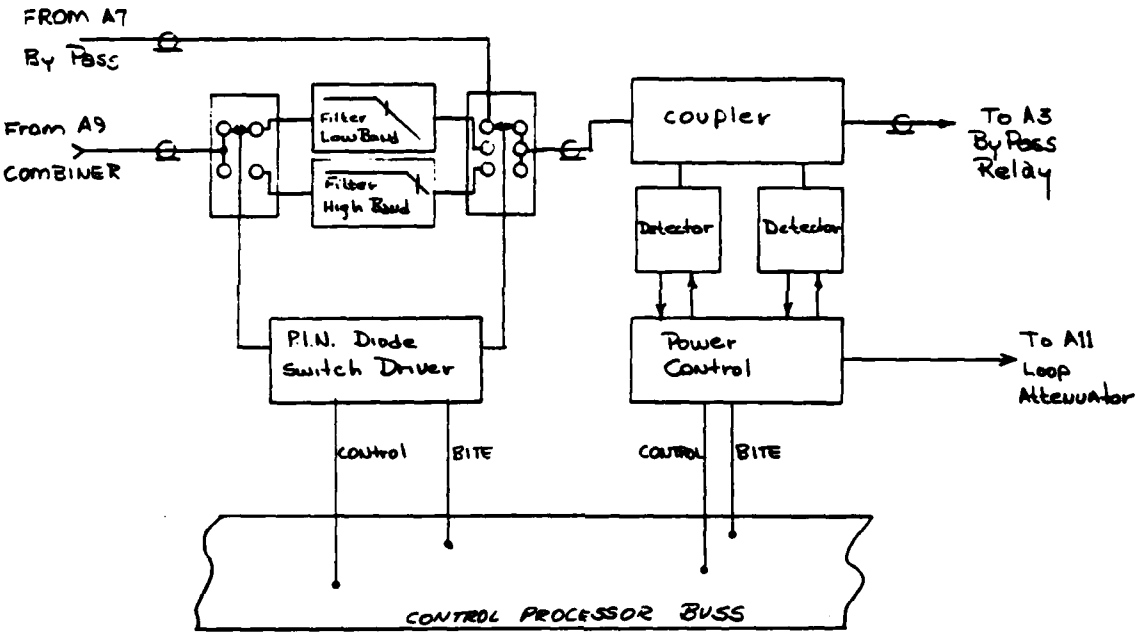


Figure 2.7-1 Harmonic Filter And Power Control Assembly

2.7.1 Low Pass Filter And Switch Assembly

The low pass filter and switch assembly includes two purchased filters: one for operation with 30-52 MHz fundamental signals and the other for the 52-88 MHz band. The input switch routes the amplifier output through either filter, while the output switch selects either a filter output or the amplifier bypass path from the RF input processor. High power series-shunt PIN diode switches select the proper RF path, and

interface circuits create the proper bias levels from TTL-compatible command inputs. To speed the switching transition times, direct pull-up or pull-down circuits to the bias supplies sequenced by a control circuit to avoid simultaneous conduction are used. Figure 2.7.1-1 is a block diagram of this circuit, and the following sections contain a detailed functional description.

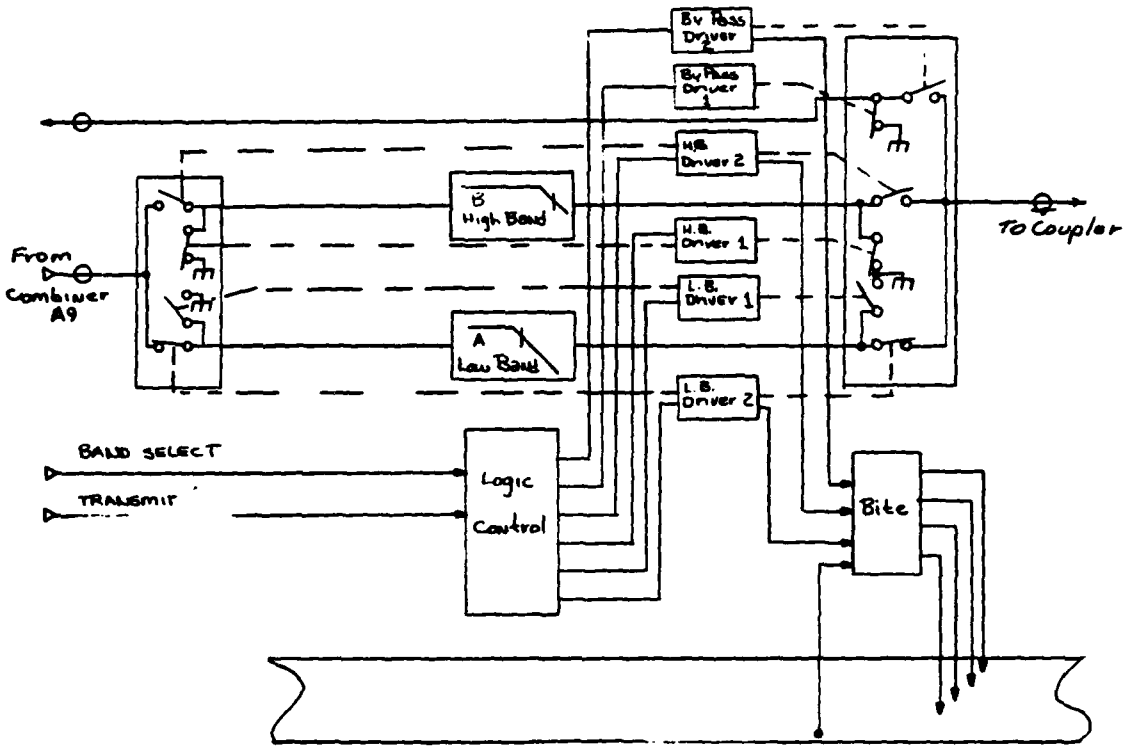


Figure 2.7.1-1 Harmonic Filter And Switch Assembly

2.7.1.1 Harmonic Filters

Both elliptic function filters with integral helical resonators used for impedance matching were purchased from Coaxial Dynamics. The results of tests performed (insertion loss, return loss and out-of-band rejection) are shown in Figures 2.7.1.1-1 through 2.7.1.1-8 for the first filters delivered.

In addition, the filters were tested under 550 watts of RF drive to evaluate their power dissipation abilities. A point in band and one at the cut-off frequency of each filter were chosen as representing the nominal and worse case power dissipation conditions. Table 2.7.1.1-1 summarizes the results and shows that the temperature rises encountered are easily manageable. Elaborate means for heatsinking the filters are not required. Mounting using standard attachment techniques will prove thermally satisfactory.

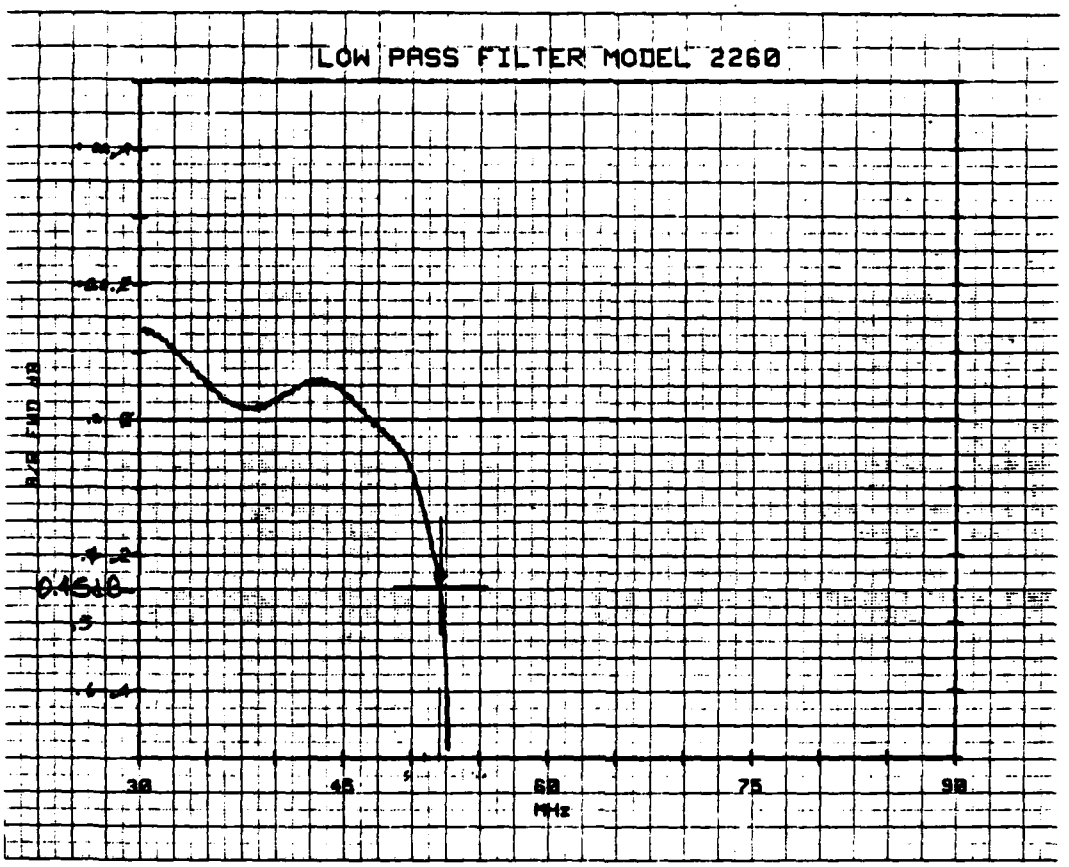


Figure 2.7.1.1-1 Low Band Filter Insertion Loss

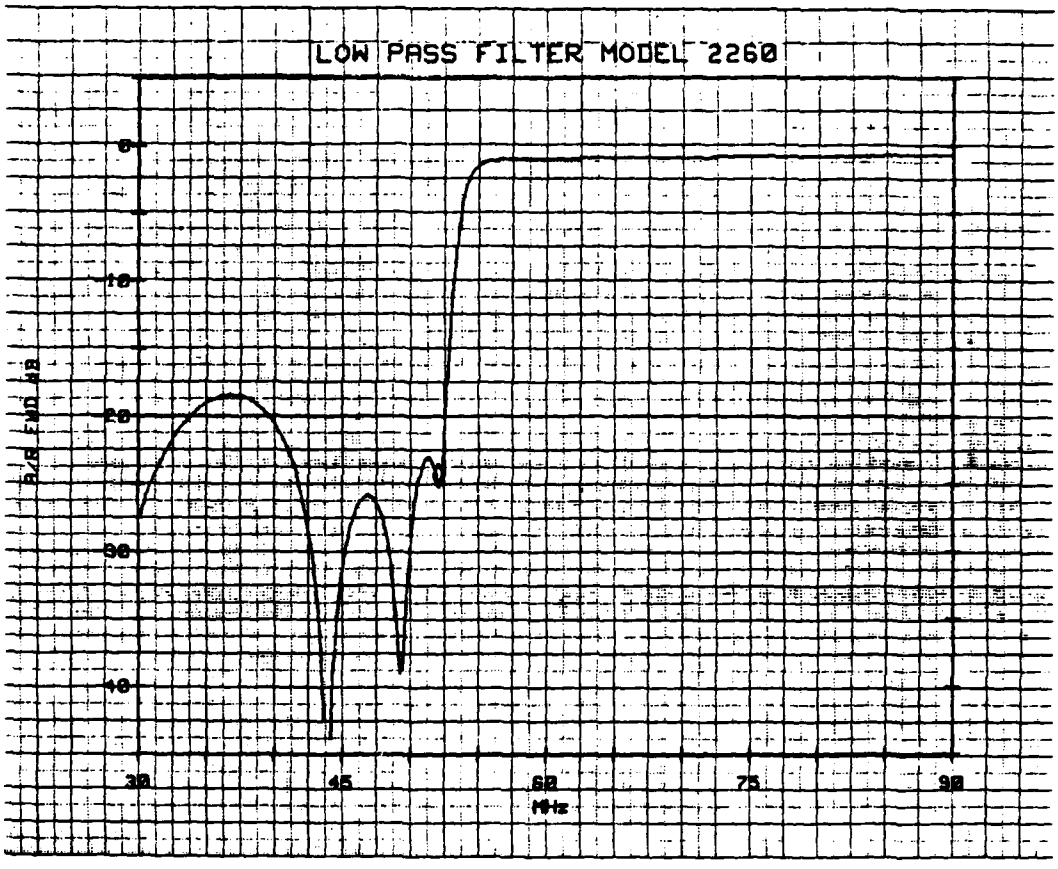


Figure 2.7.1.1-2 Low Band Filter Return Loss

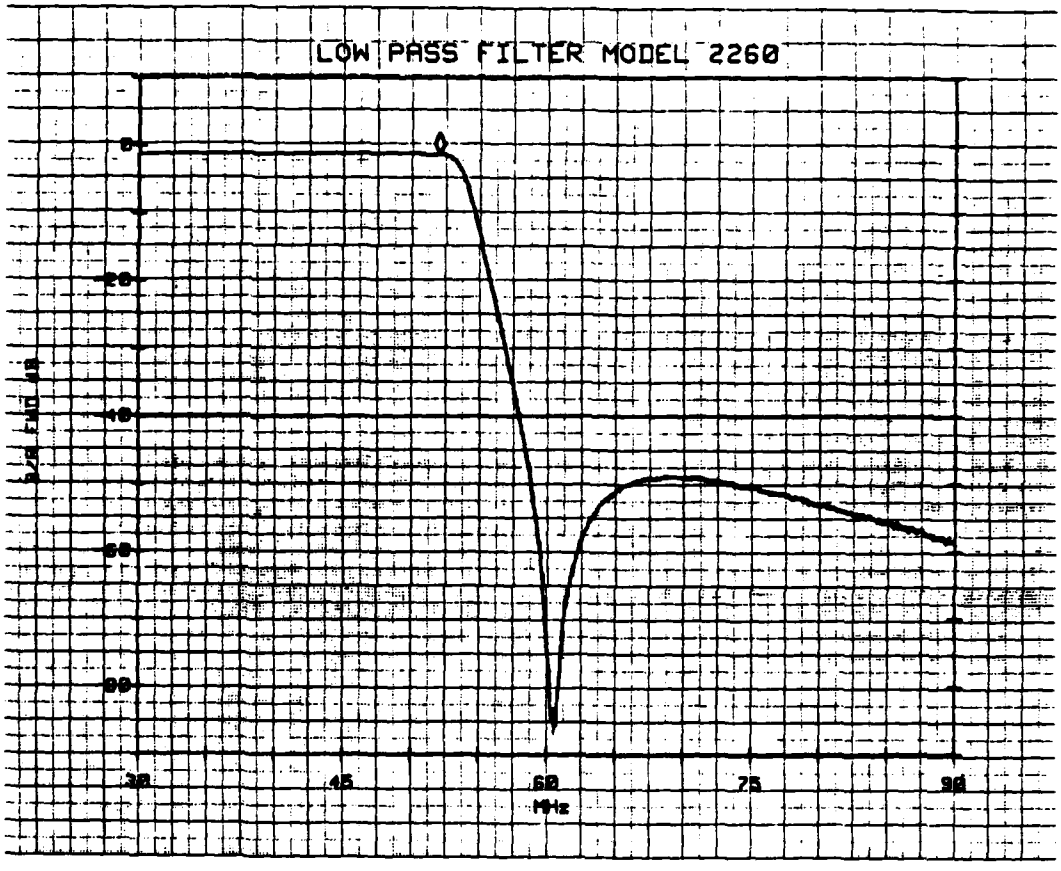


Figure 2.7.1.1-3 Low Band Filter Out-Of-Band Rejection

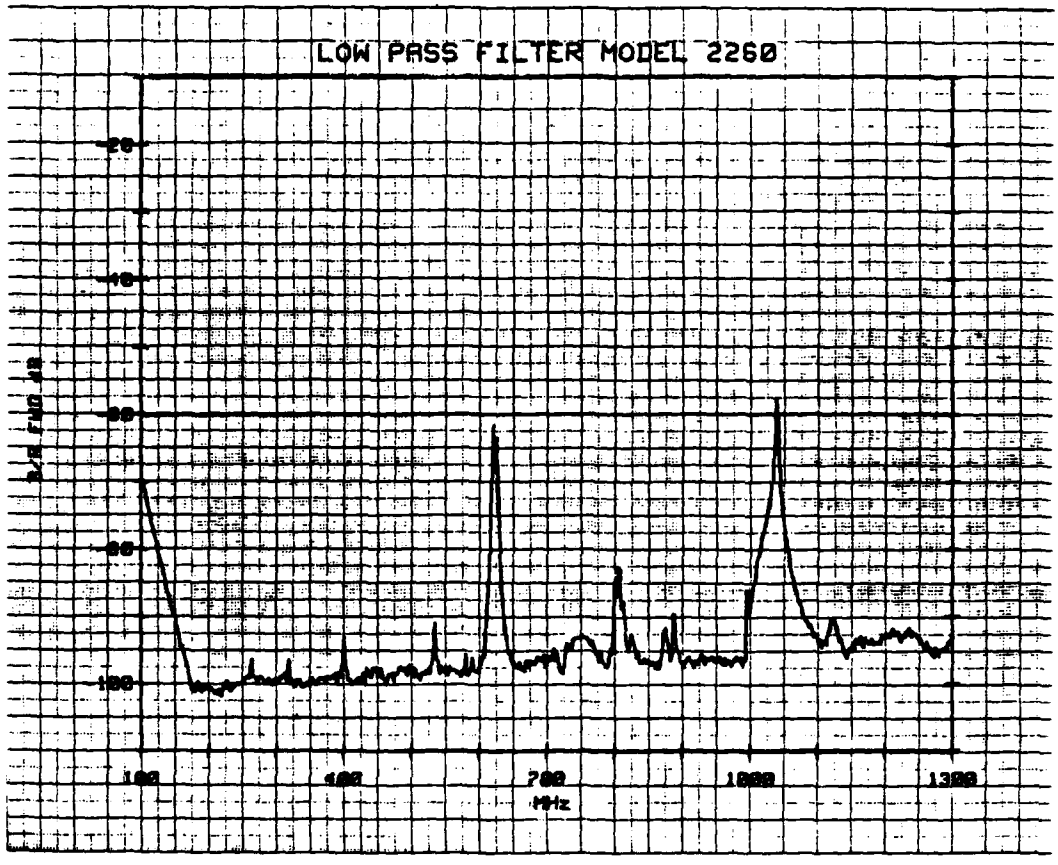


Figure 2.7.1.1-4 Low Band Filter Wide-Band Response

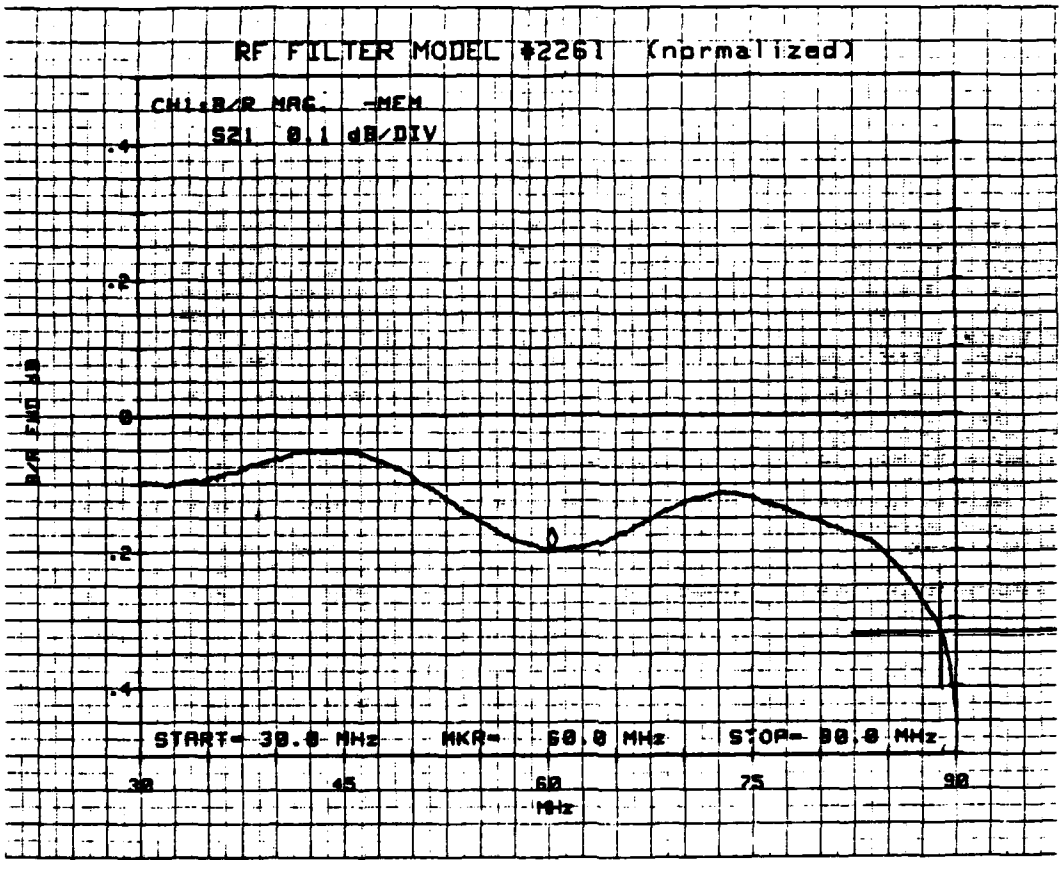


Figure 2.7.1.1-5 High Band Filter Insertion Loss

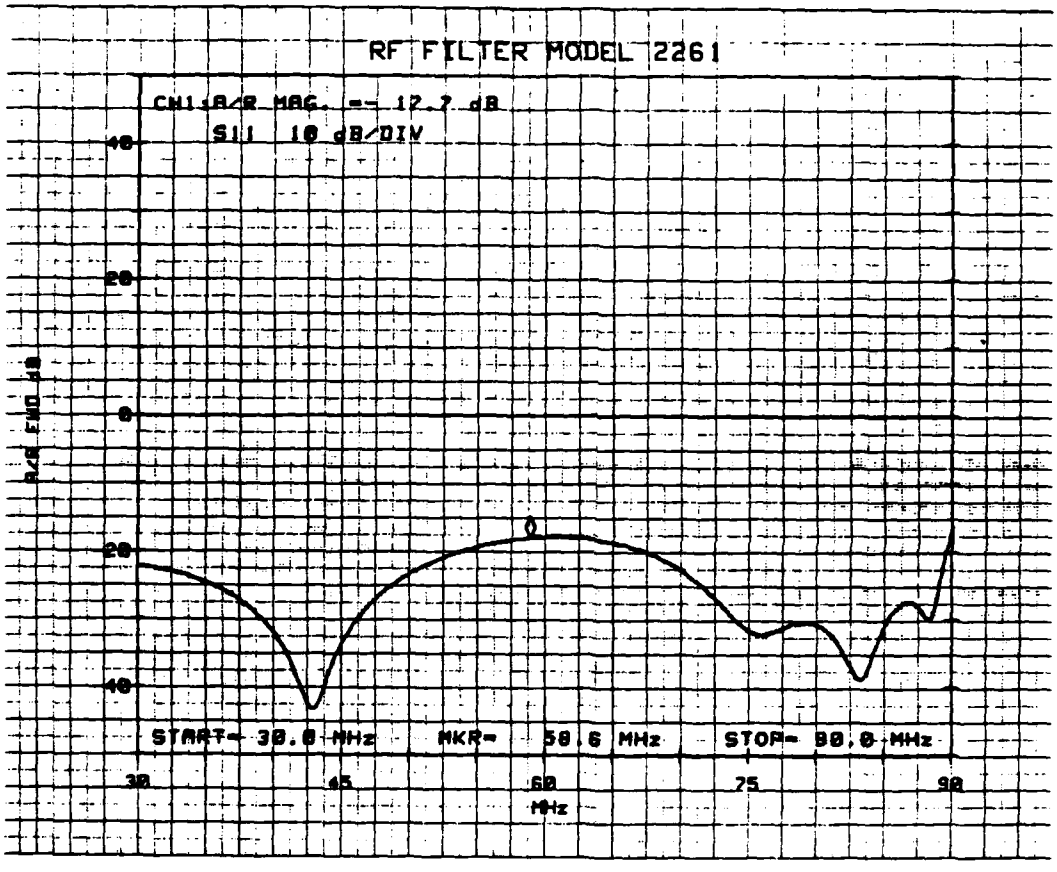


Figure 2.7.1.1-6 High Band Filter Return Loss

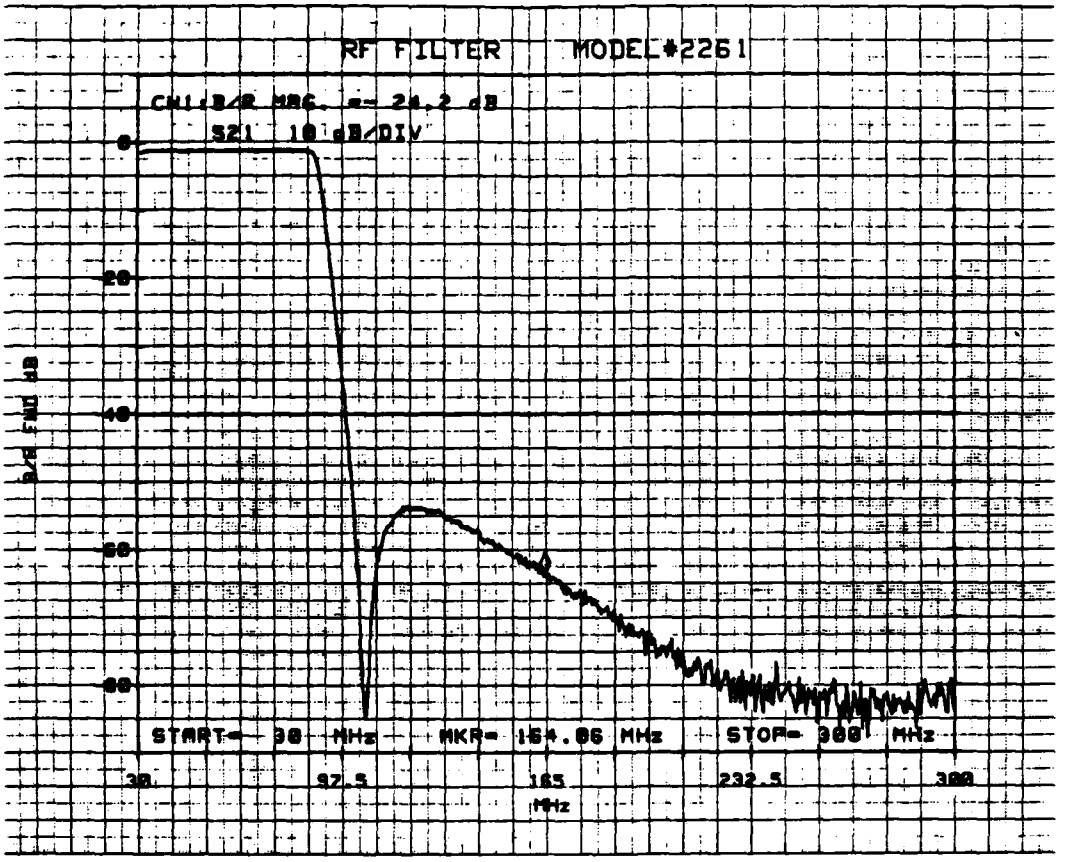


Figure 2.7.1.1-7 High Band Filter Out-Of-Band Rejection

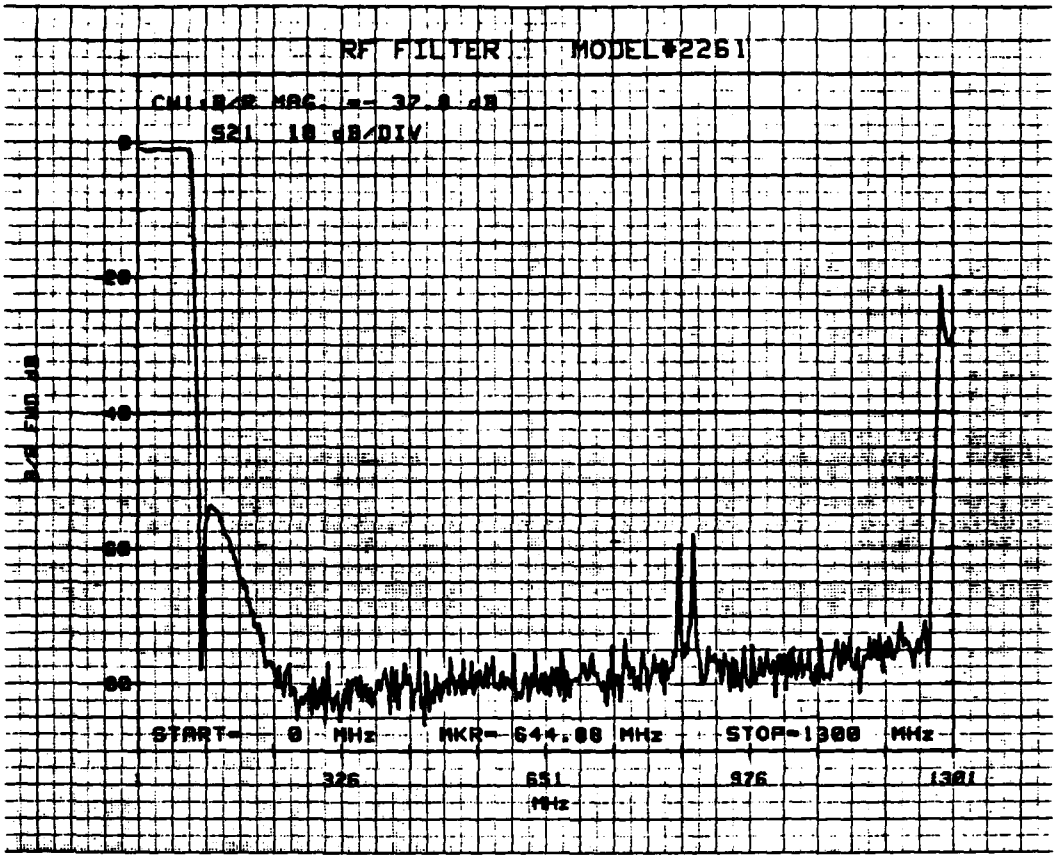


Figure 2.7.1.1-8 High Band Filter Wide-Band Response

Table 2.7.1.1-1 Harmonic Filter Temperature Versus Frequency

TEMPERATURE RISE (^{o}C) FROM BASE PLATE

	FREQUENCY (MHz)			
	LOW BAND FILTER		HIGH BAND FILTER	
TIME (MINUTES)	30	52	60	80
5	0	0	0	2.0
10	0	3.7	0	1.6
15	1	2.0	1	1.3

2.7.1.2 PIN Diode Switch Driver

Figure 2.7.1.2-1 is a block diagram of the PIN diode switch driver and logic decoder. Two commands, band select and transmit/receive, are decoded and routed to exercise the appropriate switches. Figure 2.7.1.2-2 is a schematic of the PIN diode switch assembly. The application of negative currents or positive voltages through the decoupling networks forward biases or reverse biases the diodes, respectively.

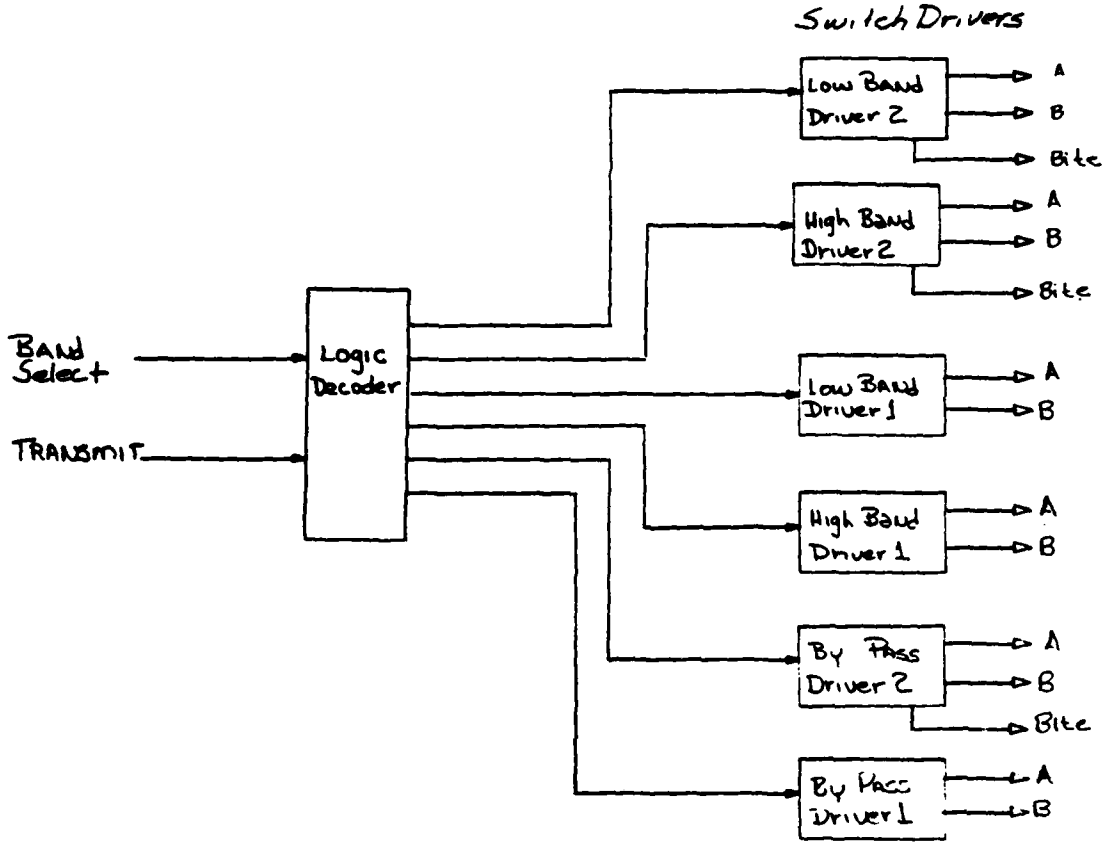


Figure 2.7.1.2-1 PIN Diode Switch Driver And Logic Decoder

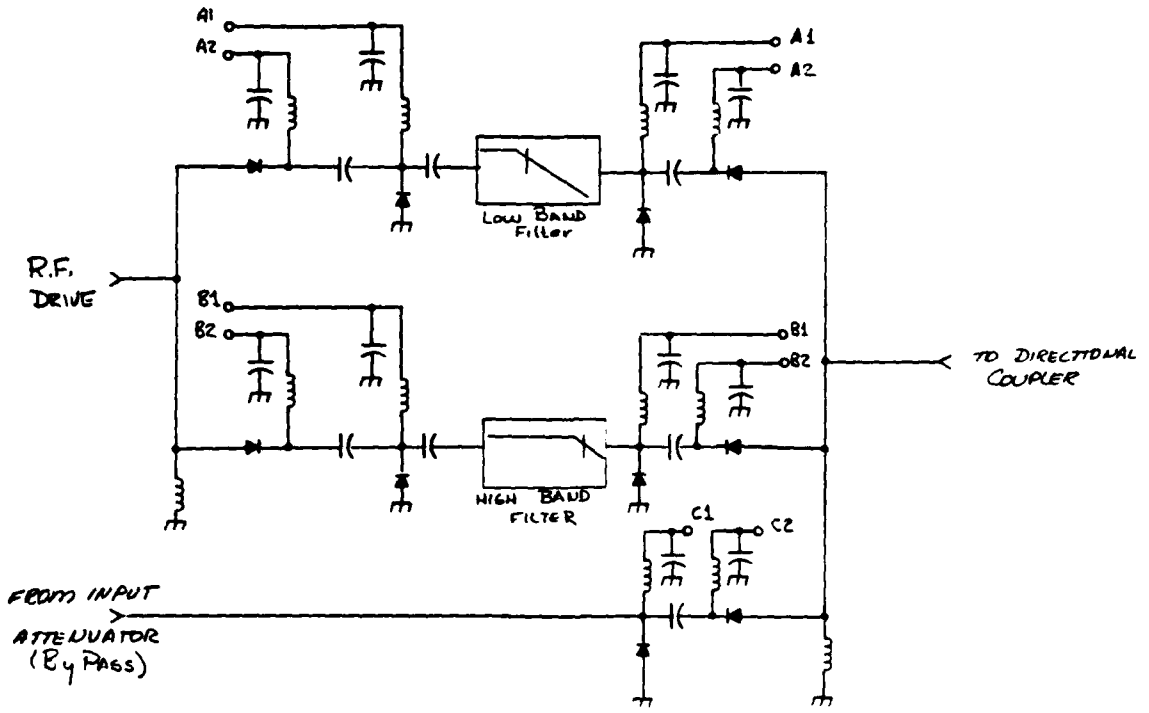


Figure 2.7.1.2-2 PIN Diode Switch Assembly

A computer model was constructed to study the isolation and loss characteristics of several diode types and networks. Figure 2.7.1.2-3 presents the theoretical limits of isolation and loss for the diodes chosen. The graph plots the equation for isolation:

$$\text{Isolation (dB)} = 10 \log \left[\left(1 + \frac{Z_o}{2R_s}\right)^2 + \frac{1}{4\pi f C_T Z_o} \left(1 + \frac{Z_o}{R_s}\right)^2 \right] \quad (2.7.1.2\text{-}1)$$

Where Z_o = Transmission line impedance
R_s = Diode series resistance
C_t = Chip and package capacitance

and insertion loss:

$$\text{Insertion Loss (dB)} = 10 \log \left[\left(1 + \frac{R_s}{2Z_o}\right)^2 + (\pi f C_T)^2 (Z_o + R_s)^2 \right] \quad (2.7.1.2\text{-}2)$$

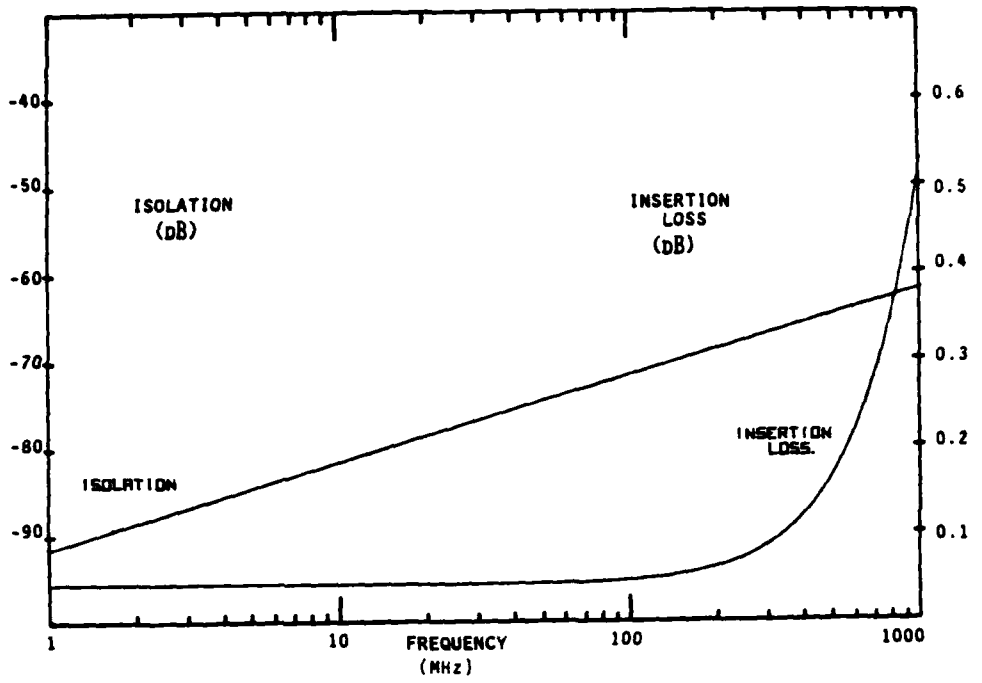


Figure 2.7.1.2-3 Theoretical Limits Of Isolation And Loss Of PIN Diode Switch

The diodes chosen have less than 0.25-ohms series resistance at the bias selected and 2.2 pF maximum capacitance.

Figure 2.7.1.2-4 is a schematic of the logic decoder. When the receive mode is selected, the switch logic ignores all other commands. A truth table is shown in Table 2.7.1.2-1. A logic 1 at the output of the decoder will command the switch driver to reverse bias the diodes by applying a high positive voltage to the cathodes. Figure 2.7.1.2-5 is a schematic of one of the six switch drivers used. A logic 0 will command the switch driver to forward bias the diodes by allowing a negative current to flow through the diodes.

To speed switching times, active pull-up and pull-down circuits are used. The logic on the input of the driver applies a precise delay to each switch transition to prevent simultaneous conduction of the output transistors. This eliminates undue stress on the output devices and increases reliability. The negative current is applied to the diode from a constant-current source that also provides a convenient point for BITE sensing. Voltage comparators are used to constantly monitor the bias for all the switches and sense the application of high voltage. The output of the comparators is interrogated periodically by the control processor to evaluate switch performance. A brassboard model of the switch driver has been built and tested from -55 degrees C to +90 degrees C. The switching times never exceed 100 microseconds for either

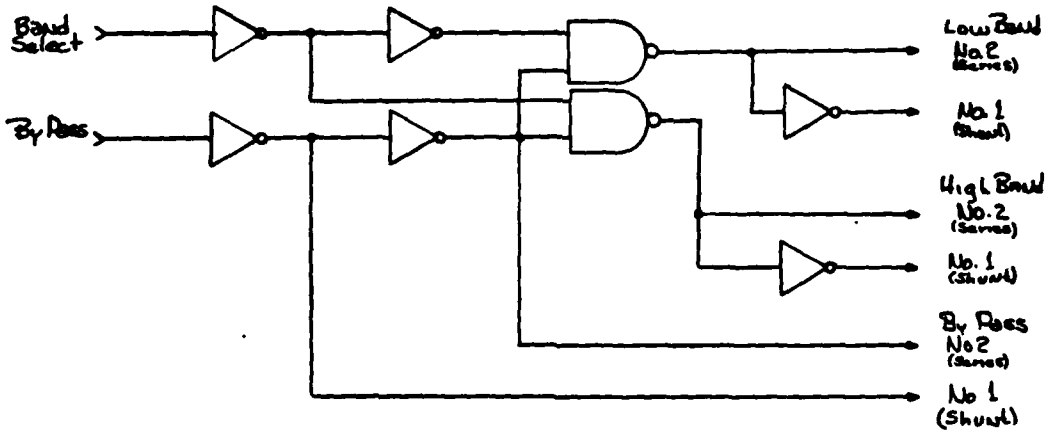


Figure 2.7.1.2-4 Switch Decoder

transition. The high current output transistor can safely dissipate the 3.6 watts required without approaching the junction temperature limits. The active devices chosen have V_{cbo} maximums exceeding twice the value of voltage used. Sufficient margin is designed into the biasing circuits to accomodate devices over the full specified range of H_{fe}.

Table 2.7.1.2-1 Switch Decoder Truth Table

BAND SELECT	RECEIVE	LOW BAND SWITCH 1	LOW BAND SWITCH 2	HIGH BAND SWITCH 1	HIGH BAND SWITCH 2	BYPASS SWITCH 1	BYPASS SWITCH 2	CONDITION
LOW	LOW	ON	OFF	ON	OFF	OFF	ON	BYPASS ENABLED
LOW	HIGH	ON	OFF	OFF	ON	ON	OFF	HIGH BAND ENABLED
HIGH	LOW	ON	OFF	ON	OFF	OFF	ON	BYPASS ENABLED
HIGH	HIGH	OFF	ON	ON	OFF	ON	OFF	LOW BAND ENABLED

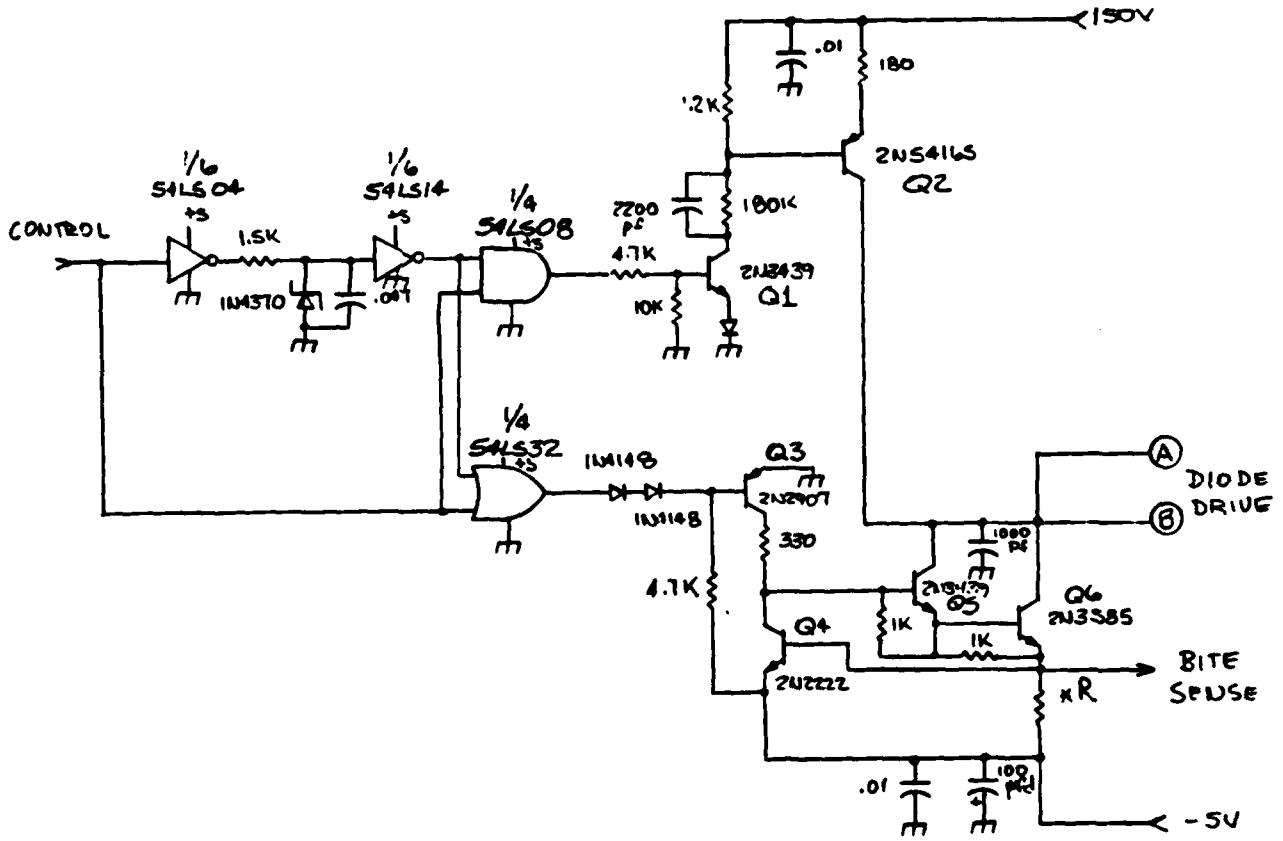


Figure 2.7.1.2-5 Switch Driver And Sequence Control Schematic

2.7.2 Output Coupler And Detector

The output coupler is implemented as a stripline backward-wave coupled line assembly with capacitively-compensated outputs to obtain a leveled output response. The circuit is built on Rogers Duroid, a low-loss controlled dielectric substrate, and is sized to obtain the desired coupling factor and to handle the power levels required.

The coupler was computer designed and optimized using SUPER-COMPACT. Originally, the design employed edge-coupled lines, but the close spacing required for -33 dB coupling (0.020") prompted the use of offset-coupled lines. With the coupled-lines separated from the through-line by a 0.031-inch layer of substrate, coupling variations due to contamination or arcing are eliminated. The active length of the coupler is 6.0 inches, the minimum length offering the desired 1.0 dB maximum peak-to-peak ripple across the 30 to 90 MHz band.

A data file listing and analysis run of the optimized coupler appear in Table 2.7.2-1. Figure 2.7.2-1 shows the electrical schematic represented in the data file. The SUPER-COMPACT data file entries account for substrate thickness, loss tangent, and dielectric constant, as well as conductor thickness and material.

Table 2.7.2-1 Directional Coupler Data File And Analysis Run

```
* VHF COUPLER WITH OFFSET COUPLED LINES
* ER=2.2 .031" BETWEEN LINES
* BETWEEN .125" LAYERS
* LINES ARE 2 OZ COPPER (2.8MIL)
*
BLK
 OCL 1 2 3 4 W=190MIL S=31MIL WC=-20MIL P=6IN SUB
 RES 3 0 R=50
 RES 4 0 R=50
FORWARD:2POR 1 2
END
LAD
 FORWARD 1 2
TRL 2 3 W=190MIL P=500MIL SUB
 TRL 3 4 W=375MIL P=250MIL SUB1
 SLC 4 0 L=2.3NH C=?255.95PF?
COUPLER:2POR 1 4
END
FREQ
 STEP 30MHZ 90MHZ 5MHZ
END
DATA
 SUB:SL B=281MIL ER=2.2 TAND=.0005 MET1=CU 2.8MIL
 SUB1:MS H=56MIL ER=2.2 TAND=.0005 MET1=CU 2.8MIL
END
OPT
 COUPLER MS21=-33DB
END
OUT
 PRI COUPLER S
END
```

```
CIRCUIT:  COUPLER
S-MATRIX, ZS =   50.0+J   0.0  ZL =   50.0+J   0.0
```

FREQ	S11		S21		S12		S22		S21
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	db
30.00000	0.008	75	0.022	29	0.022	29	0.776	-141	-33.01
35.00000	0.009	71	0.023	23	0.023	23	0.822	-145	-32.59
40.00000	0.010	68	0.024	18	0.024	18	0.858	-149	-32.32
45.00000	0.011	64	0.025	13	0.025	13	0.885	-152	-32.17
50.00000	0.012	61	0.025	9	0.025	9	0.906	-155	-32.09
55.00000	0.014	57	0.025	5	0.025	5	0.922	-157	-32.08
60.00000	0.015	54	0.025	1	0.025	1	0.935	-159	-32.11
65.00000	0.016	51	0.025	-2	0.025	-2	0.946	-161	-32.18
70.00000	0.017	47	0.024	-5	0.024	-5	0.954	-162	-32.29
75.00000	0.017	44	0.024	-8	0.024	-8	0.961	-164	-32.43
80.00000	0.018	41	0.023	-11	0.023	-11	0.967	-165	-32.60
85.00000	0.019	37	0.023	-14	0.023	-14	0.972	-166	-32.80
90.00000	0.020	34	0.022	-16	0.022	-16	0.976	-167	-33.02

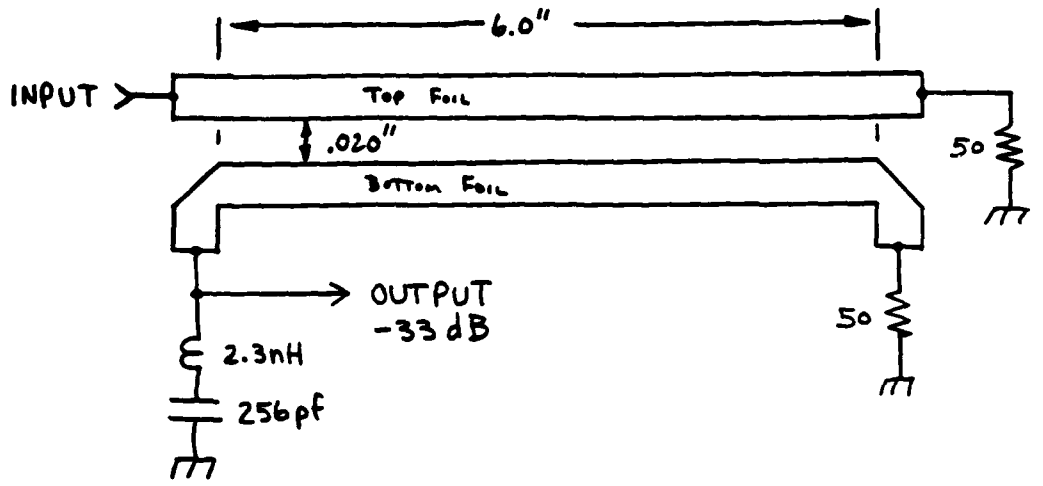


Figure 2.7.2-1 Schematic Of Coupler Represented In Data File

Although designed and modeled as a single-directional coupler, the actual coupler is dual-directional, consisting of two coupled lines oriented on opposite sides of the through-line, and in opposite directions. The three 2-ounce copper 50-ohm lines are etched onto a single 0.031-inch Duroid PCB. The through-line is centered on the top surface, with the coupled lines below. The offset-coupled stripline PCB is mounted between two 0.125-inch Duroid sheets, and compressed between two aluminum plates to form a stripline assembly. Table 2.7.2-2 is a list of measured data from a breadboard dual-directional coupler. The measured worst case directivity is 30.8 dB.

Table 2.7.2-2 Directional Coupler Data

FREQ (MHz)	30	45	60	75	90
FORWARD PORT	-32.9	-32.1	-32.0	-32.3	-32.9
REVERSE PORT	-32.8	-32.0	-31.9	-32.1	-32.5

The RF detector converts the signal sampled by the -33 dB directional coupler to a differential DC voltage for power monitor and control functions. Represented schematically in Figure 2.7.2-2, the detector features a bifilar transformer and full-wave Schottky rectifier, allowing a much smaller filter capacitor and a much wider bandwidth than a half-wave rectifier. The detector diodes are biased for maximum dynamic range and VSWR accuracy, and the temperature compensation diode offsets the quiescent differential output to zero volts. Table 2.7.2-3 shows the DC output voltage from the breadboard coupler/detector versus temperature and frequency at 100 watts forward power.

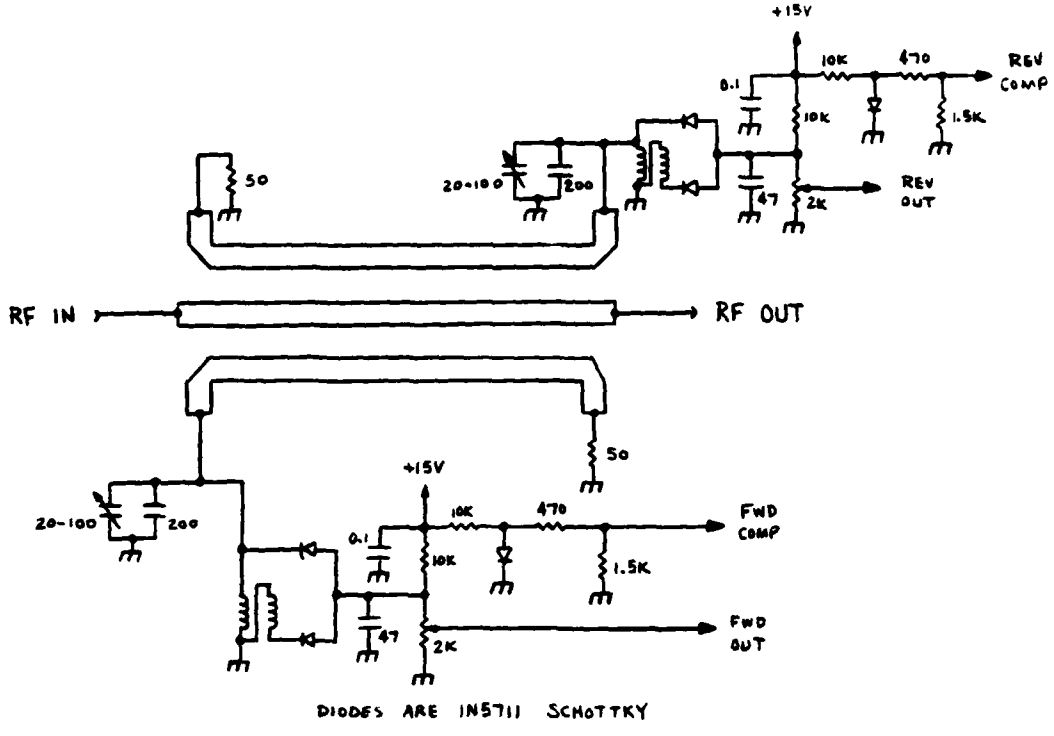


Figure 2.7.2-2 Directional Coupler/Detector Schematic

Table 2.7.2-3 Coupler/Detector Differential Output Voltage Versus Temperature (P_{FWD} = 100 W)

TEMPERATURE (^{o}C)	FREQUENCY (MHz)				
	30	45	60	75	88
-50	-1.39	-1.50	-1.40	-1.46	-1.38
+25	-1.36	-1.48	-1.37	-1.46	-1.38
+85	-1.32	-1.46	-1.31	-1.44	-1.39

2.7.3 Loop Amplifier And Summing Network

The schematic diagram for the loop amplifier and summing network is shown in Figure 2.7.3-1. The summing network is designed so that:

$$E_{ref} = (E_f - E_{fc}) + 0.22\ (E_r - E_{rc}) \qquad (2.7.3\text{-}1)$$

Where E_{ref} = Loop reference voltage

E_f = Forward power detector output voltage

E_{fc} = Forward power detector temperature compensation output

E_r = Reflected power detector output voltage

E_{rc} = Reflected power detector temperature compensation output

The feedback forces the RF power level to the point where the detector outputs satisfy the above equation.

The loop amplifier is designed for 60 dB open-loop gain and can generate loop control voltages from -14.8 VDC to +6.6 VDC. The output impedance is very low over the entire output range so that the loop amplifier can drive the RF bypass networks on the gates of the FET driver without significantly affecting the loop frequency response.

Calculations were made to ensure that none of the breakdown voltages for the CA3045 ICs are exceeded for any possible combination of input levels. The 1.8-kilohm resistors in the current source lines prevent the maximum Vce from being exceeded on the current source transistors. The 1.8-kilohm resistor in the power supply line to the first differential amplifier prevents its maximum Vce from being exceeded and the 560-ohm resistor protects the level shift transistor. Calculations were also made to be sure that all collector-substrate junctions remain reverse biased for any possible combination of input levels.

The following procedure was used to find the uncompensated open-loop response. First, the phase/gain data from FET control input to detector output was taken using a low-frequency network analyzer. The detector load was set to 2200 ohms, which is the input impedance of the loop amplifier. Since these measurements were made relative to the FET control input, they had to be modified to account for the reaction of the loop amplifier output impedance with the FET control input impedance. The loop amplifier output impedance was measured by temporarily loading the loop amplifier with a large capacitance (0.1 uF) and measuring the 3 dB corner frequency. The loop amplifier output impedance was found to be approximately 17 ohms. Next, the equivalent network looking into the FET control input was analyzed using the SUPER-COMPACT program for the circuit of Figure 2.7.3-2.

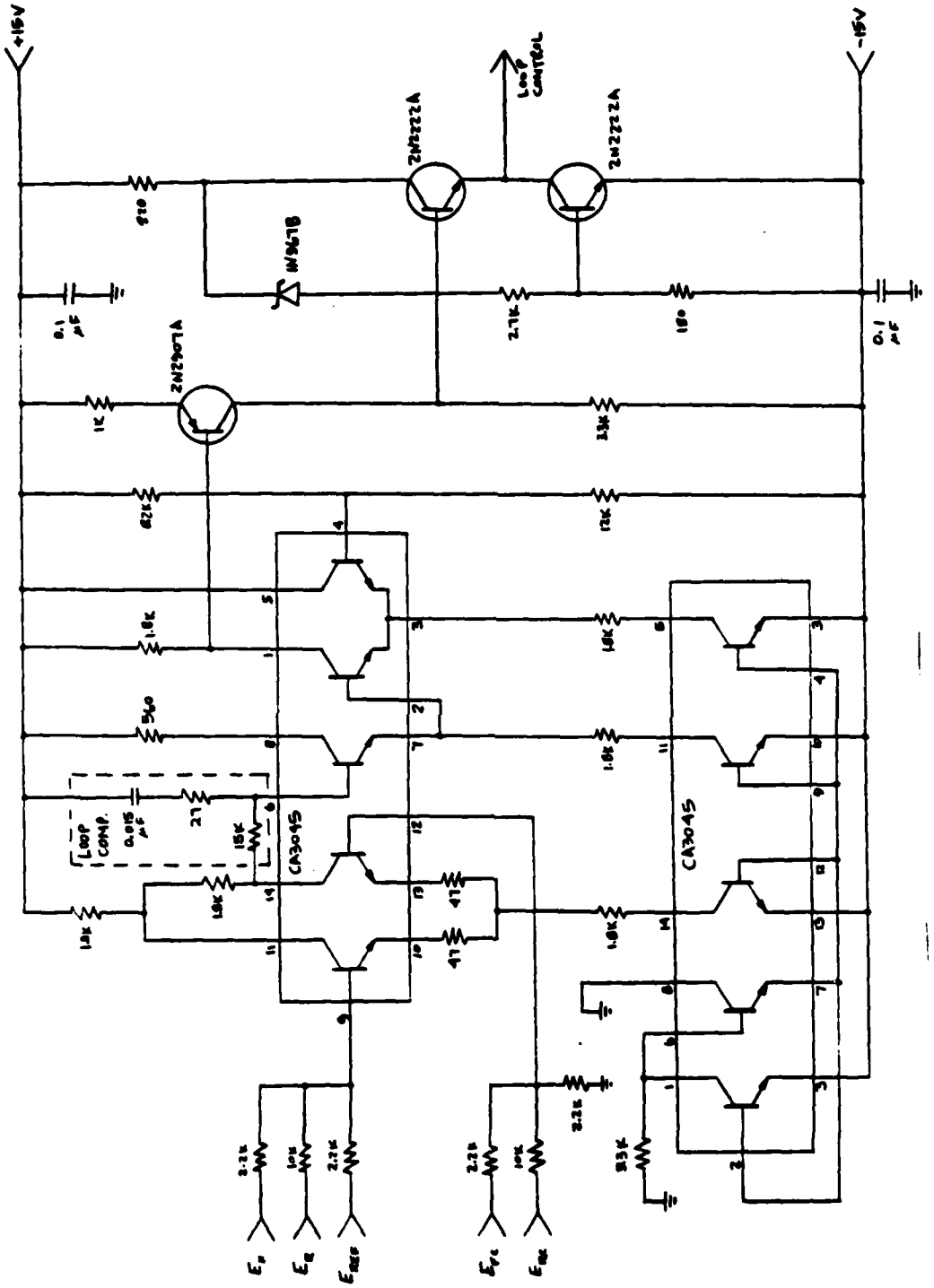


Figure 2.7.3-1 Loop Amplifier And Summing Network Schematic

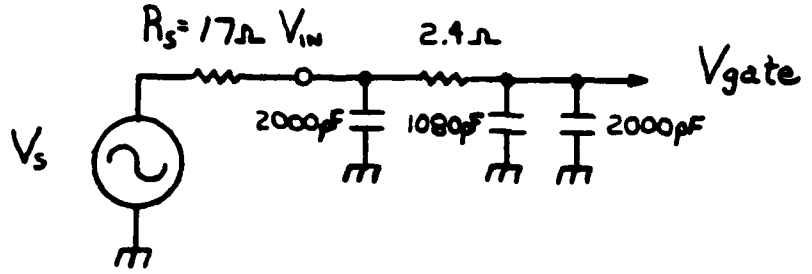


Figure 2.7.3-2 FET Control Input Model

The SUPER-COMPACT program calculated the magnitude and phase of V_{gate}/V_s and V_{gate}/V_{in}, from which V_{in}/V_s was obtained. Next, phase and gain data were measured on the uncompensated loop amplifier, using the low-frequency network analyzer. Then the three sets of data (the uncompensated loop, V_{in}/V_s, and V_{det}/V_{in}) were combined to obtain the the overall uncompensated loop response. The uncompensated open-loop response is shown in Figure 2.7.3-3.

The gain and phase of the following transfer function closely matches the uncompensated open-loop response.

$$H(j,f) = \frac{K}{\left(1 + \frac{f}{f_{p1}}\right)\left(1 + \frac{f}{f_{p2}}\right)\left(1 + \frac{f}{f_{p3}}\right)} \cdot e^{j180^0} \qquad (2.7.3\text{-}2)$$

Where f_{p1} = 540 kHz
f_{p2} = 4 MHz
f_{p3} = 6.5 MHz
and K = 794.33 (58 dB)

Therefore, this function was used to model the uncompensated open-loop response.

From Figure 2.7.3-3, at 180 degrees of phase change, the gain is 46 dB. Thus, for 10 dB of gain margin, 56 dB of attenuation was needed at 1.6 MHz. The following compensation network (Figure 2.7.3-4) was used to achieve the required high-frequency attenuation while not contributing significantly to the high-frequency phase shift.

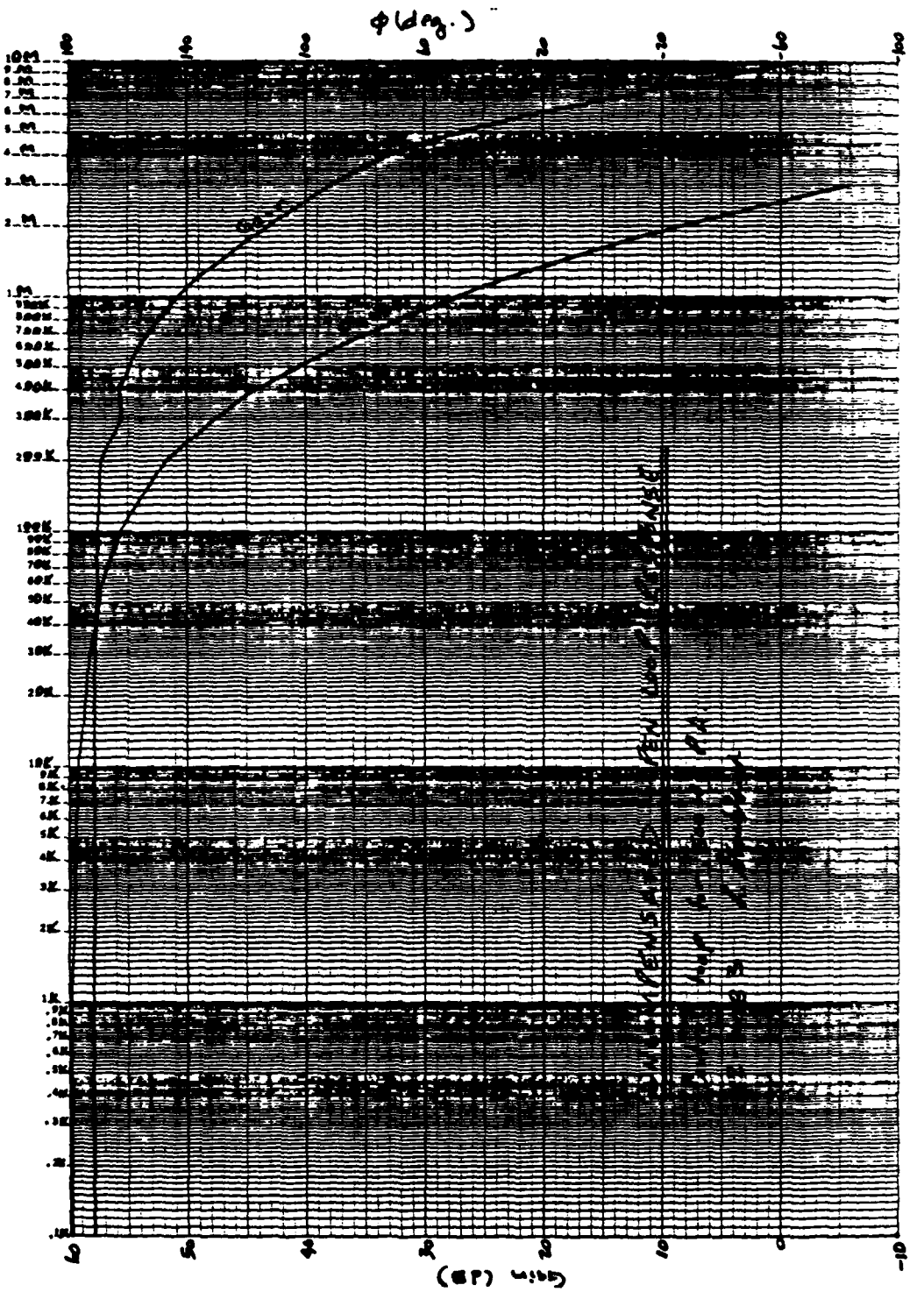


Figure 2.7.3-3 Open-Loop Uncompensated Response

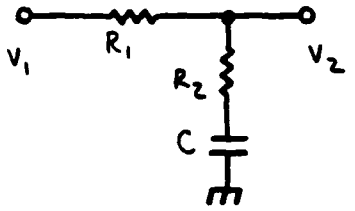


Figure 2.7.3-4 Control Loop Compensation Network

The transfer function for this network is:

$$\frac{V_2}{V_1}(jf) = \frac{1 + j\frac{f}{f_z}}{1 + j\frac{f}{f_p}} \qquad (2.7.3\text{-}3)$$

Where $$f_z = \frac{1}{2\pi C R_2} \qquad (2.7.3\text{-}4)$$

and $$f_p = \frac{1}{2\pi C(R_1 + R_2)} \qquad (2.7.3\text{-}5)$$

At very high frequencies, the attenuation provided by this network is:

$$\frac{V_2}{V_1} = \frac{R_2}{R_1 + R_2} \qquad (2.7.3\text{-}6)$$

which is also the ratio f_p/f_z.

Therefore, setting $$\frac{R_2}{R_1 + R_2} = -56 \text{ dB} \qquad (2.7.3\text{-}7)$$

then $f_p = 0.0016\ f_z$.

The transfer function for the uncompensated loop response and the transfer function for the compensation network are then combined to find the compensated open-loop response. Several values of pole and zero frequencies were tried for the compensation network transfer function, keeping $f_p = 0.0016\ f_z$. The results are plotted in Figure 2.7.3-5, and summarized in Table 2.7.3-1.

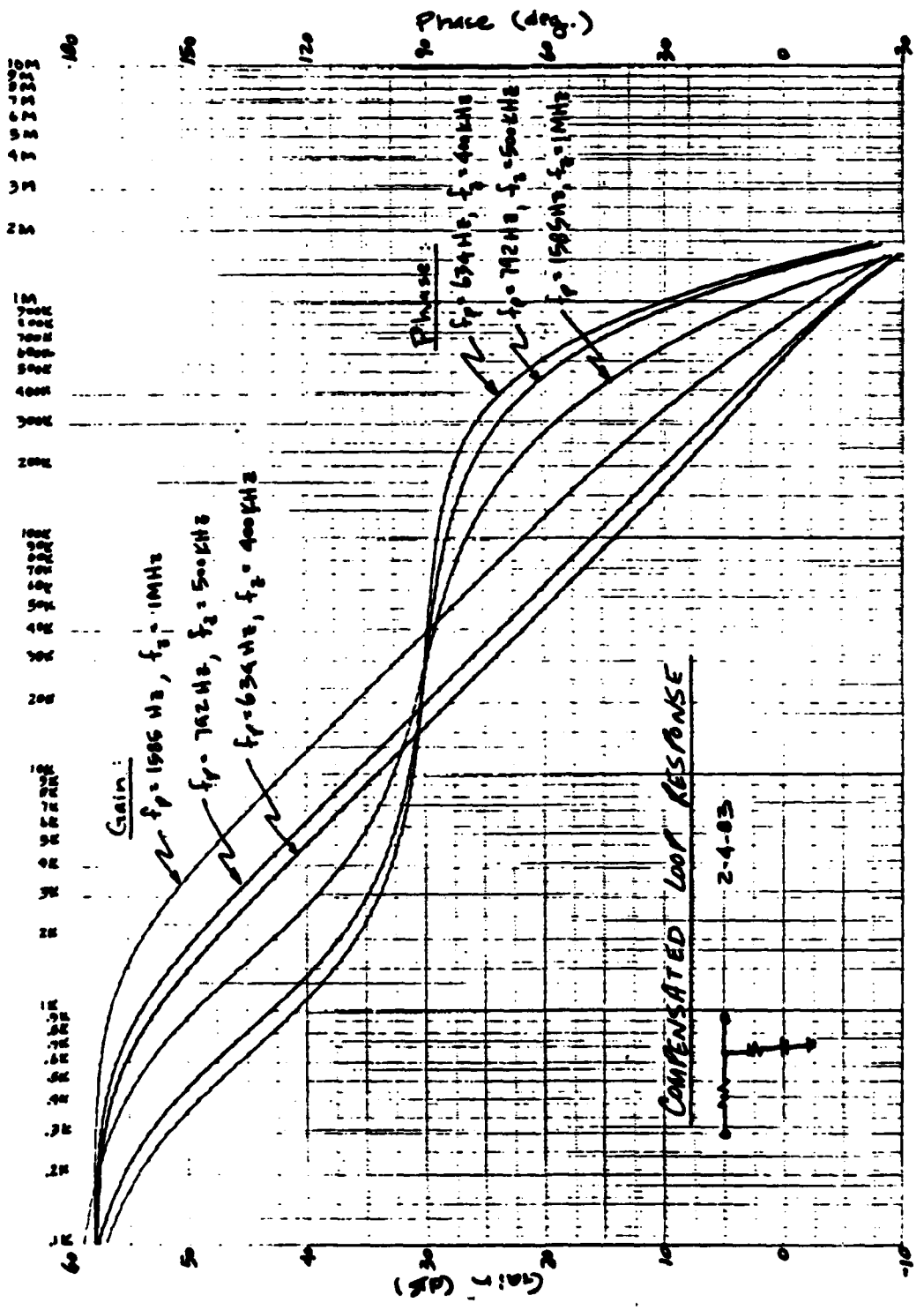


Figure 2.7.3-5 Compensated Control Loop Response

Table 2.7.3-1 Loop Compensation

POLE FREQUENCY (Hz)	ZERO FREQUENCY (kHz)	GAIN MARGIN (dB)	PHASE MARGIN (Degrees)
1585	1000	4	18
792	500	8	50
634	400	9	60

Setting R_1 = 16.8 kilohms (1800-ohm source plus 15-kilohm resistor) and f_p = 634 Hz, then R_2 = 26.67 ohms and C = 0.01492 uF. Using R_2 = 27 ohms and C = 0.015 uF, f_p = 603.6 Hz and f_z = 393 kHz.

The open-loop response resulting from the use of these values in the compensation network transfer function is shown in Figure 2.7.3-6. This plot shows that the design has 8.3 dB of gain margin and 58 degrees of phase margin while maintaining a gain of 26 dB at 25 kHz.

The following compensation network (Figure 2.7.3-7) was also tried.

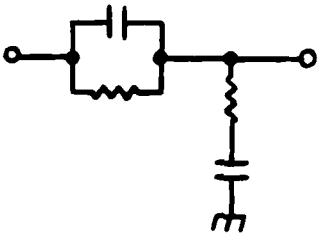


Figure 2.7.3-7 Alternate Compensation Network

It was found that this network could provide a small advantage in gain and phase margin over the previous one, but not enough to justify an extra part. Therefore, the earlier compensation network is used.

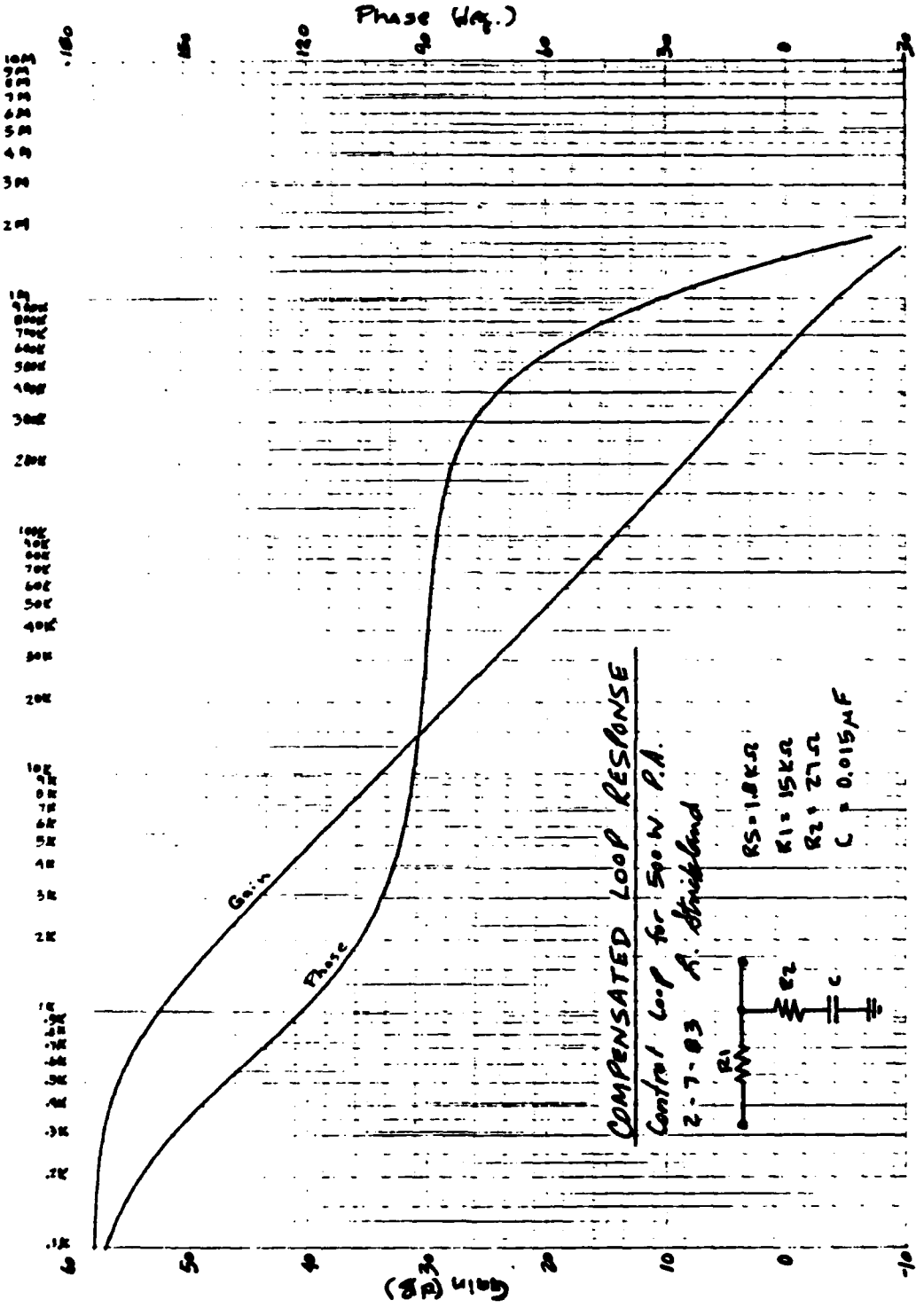


Figure 2.7.3-6 Compensated Loop Response

2.7.4 Loop Reference Generator

The schematic diagram of the loop reference generator is shown in Figure 2.7.4-1 along with some monitoring circuits that are described in the next section. The basic reference voltage is generated with a precision voltage regulator and is then modified based upon the frequency of the input RF signal and the desired output power level.

A uA723 is used to generate the basic reference voltage. This circuit employs feedback around a high gain buffer amplifier in order to maintain an output voltage equal to the voltage established across a temperature compensated zener diode. The temperature coefficient of the output voltage is typically 0.002%/^{o}C, or 0.015%/^{o}C worst case. This means that if the output power is set to 500 watts at 25 degrees C, it will typically vary by 2 watts over temperature, the worst case variation being 15 watts. These variations are due to the temperature coefficient of the basic reference alone; they do not include variations due to the rest of the reference generator.

The output of the precision regulator is fed into two cascaded multiplying digital-to-analog converters. The first multiplying D/A modifies the basic reference in order to compensate for variations in detector outputs due to frequency. A digital word sent by the processor makes the appropriate modification based upon the frequency of the RF input signal. The second multiplying D/A further modifies the reference according to the desired output power. Another digital word is supplied by the processor to this D/A in order to scale the reference by the proper value.

The multiplying D/A's do not supply an output voltage directly. They sink a current proportional to the input reference voltage scaled by the digital word. This current must be converted back to a voltage. Operational amplifiers are used to accomplish this conversion. These op-amps also buffer the various progressions of the loop reference voltage from loads in the monitoring circuits.

Eight-bit latches are used to store the frequency correction word and the power level word. The latches are enabled independently so that they can share the same eight-line bus. Six of these lines are also shared by the output information from the monitoring circuits.

No experimental data is presented for the loop reference generator since the breadboard for this circuit is now under construction. Data for this circuit will be presented in the next quarterly report.

2.7.5 Power Control Monitoring Circuits

Figure 2.7.4-1 also shows the schematic diagram for the power control monitoring circuits. These circuits provide the processor with the following information: forward and reflected peak power levels, VSWR,

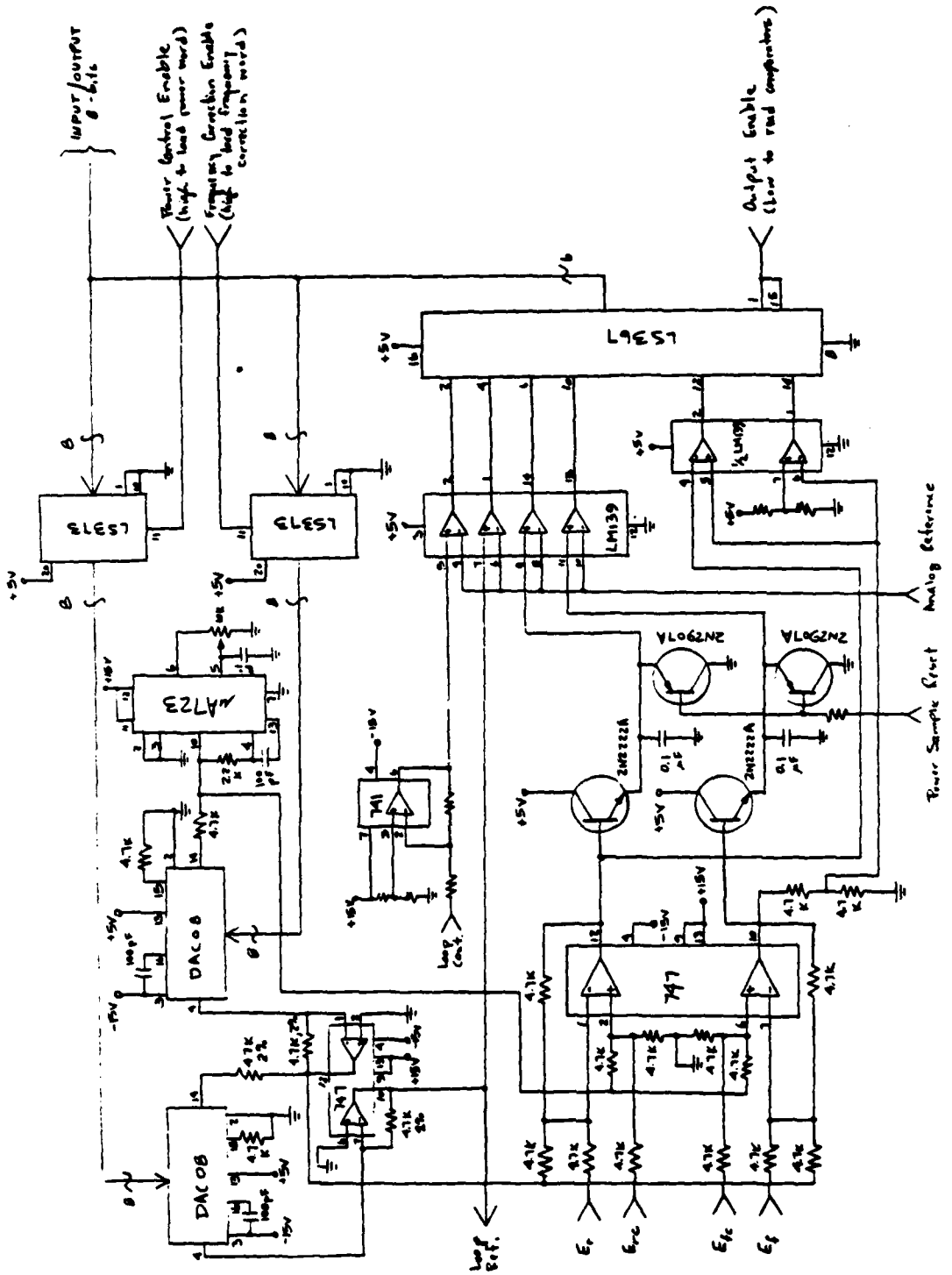


Figure 2.7.4-1 Loop Reference Generator And Power Control Monitoring Circuits

loop control voltage, and loop reference voltage. There is also a circuit that notifies the processor if the output power exceeds 575 watts.

The output voltage from the forward power sampling detector, along with its temperature compensation output, is fed into a summing network and operational amplifier. Also fed into this network are the raw loop reference and the frequency compensated loop reference. The summing network is configured so that the operational amplifier output is equal to the forward power sampling detector output corrected for frequency and temperature. An identical summing network and operational amplifier perform the same operation on the reflected power sampling detector output. Thus, at the outputs of these operational amplifiers are frequency- and temperature-independent voltages proportional to the forward and reflected RF signals.

These frequency- and temperature-independent voltages are fed into peak sample-and-hold circuits, each consisting of one NPN and one PNP transistor and a 0.1 uF, low-leakage, sample-and-hold capacitor. The NPN transistor turns on whenever its base voltage rises, charging the capacitor to a voltage level 0.7 V below the NPN base voltage. If the level at the base of the NPN drops, the NPN turns off since its emitter voltage is held constant by the capacitor. The capacitors are discharged only when the processor drops the power sample reset line low, turning the PNP transistors ON. Thus, these circuits retain a voltage proportional to peak forward and reflected RF power that occurs between each power sample reset pulse. The voltages thus retained are compared with an analog reference supplied by the processor.

The analog reference is also compared with the loop reference voltage and a signal proportional to the loop control voltage. Since the loop control voltage is between +6 and -15 VDC, and since the analog reference is between 0 and +5 VDC, a scaling and offset of the loop control voltage is necessary before comparing it to the analog reference. The scaling and offset of the loop control voltage is accomplished by an operational amplifier configured as shown in Figure 2.7.5-1.

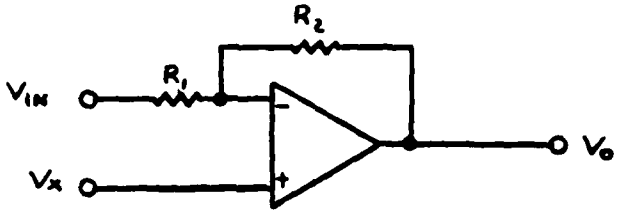


Figure 2.7.5-1 Loop Control Voltage Scaling And Offset Circuit

For this circuit,

$$V_o = V_{in} \frac{-R_2}{R_1} + V_R \frac{(R_2 + 1)}{R_1} \qquad (2.7.5\text{-}1)$$

Making $R_1/R_2 = 4.2$ and $V_x = 1.155$ VDC, then

$$V_o = \frac{-V_{in}}{4.2} + 1.43 \qquad (2.7.5\text{-}2)$$

from which the following chart is derived:

V_{in}	V_o
-15	5.00
-10	3.81
- 5	2.62
0	1.43
+6	0.00

Note that there is an inversion, but this can be corrected for by connecting the output thus obtained to the inverting input of the comparator and the analog reference to the non-inverting input.

The voltage proportional to the square root of the forward RF signal power is divided in half and compared to the voltage proportional to the square root of the reflected RF signal power. When the reflected voltage becomes greater than one-half the forward voltage, this comparator switches state indicating a VSWR greater than 3:1. Also, when one-half the forward power exceeds 287.5 watts, another comparator trips indicating an overpower condition.

The information from all the comparators described thus far is transferred to the processor when the processor enables the 54LS367 buffer circuit.

The power control monitoring circuits are still in the planning stages. No breadboard exists as yet and some part values remain undetermined. An analysis needs to be done in order to determine if the diode drops in the peak sample-and-hold circuits will cause a problem, especially over temperature.

2.8 RF INPUT PROCESSOR (A7)

After passing through the RF fail-safe mechanical relay assembly (A3), the RF input processor performs the initial modification of the characteristics of the input signal. The primary function of this module is to attenuate the wide-ranging input signal level to sub-bands at a maximum level compatible with the RF drive amplifier (A11) and to detect and count the frequency of the RF drive signal. Figure 2.8-1 is a block diagram of the module.

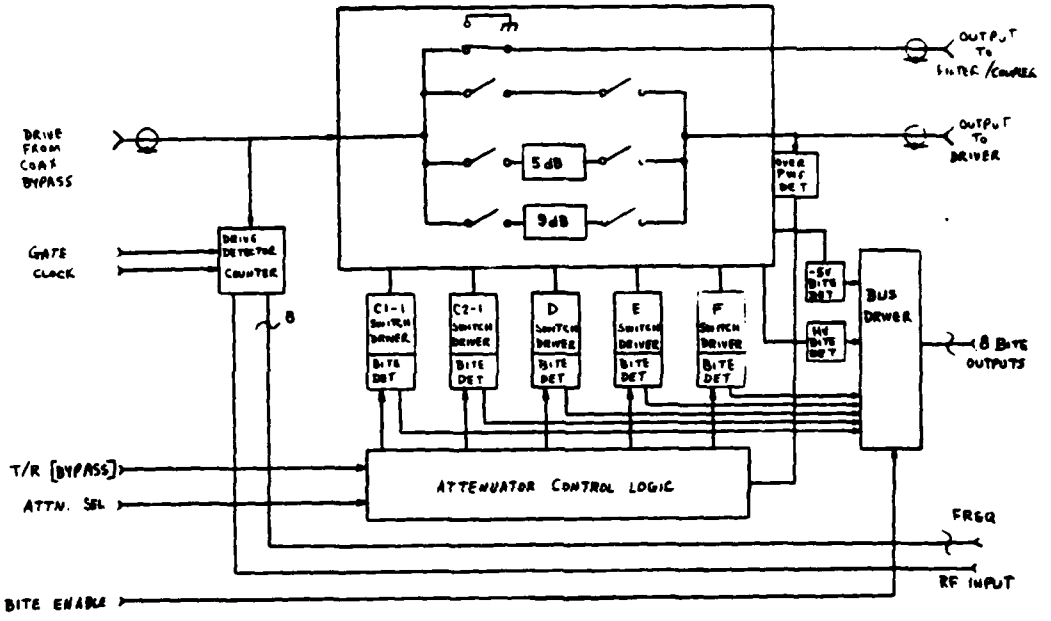


Figure 2.8-1 RF Input Processor Block Diagram

The driver signal is first passed through an electronic PIN diode switch assembly where it is routed to one of four paths, either the RF bypass to the amplifier output or to one of the three attenuator sections. A sample of the input signal is also routed through an attenuator and buffer amplifier to a frequency counter and level detector. The selected attenuator output is finally routed through an output switch and connected to the variable gain driver amplifier.

The input processor switches one of two fixed attenuators or, at low drive levels, a through connection into the input RF path according to the drive level present. The selected attenuator is normally the highest attenuation, but is reduced to a lower level by the processor if the full output is not achieved after a short time delay. After switching to a lower level, that level is maintained as long as power is applied unless

the input suddenly increases. A hardware reset, driven by a detector on the module output, increases attenuation when drive levels increase beyond a predetermined threshold (approximately 12 watts at the module output).

The attenuation selected is monitored by the control processor via the BITE in addition to the frequency and input level to the power amplifier.

Because of the power dissipation under high input drive power levels, an integral heatsink conducts heat from the attenuators to the finned case.

2.8.1 Diode Switch Assembly

The diode switch assembly uses five switch drivers similar to those used in the filter/directional coupler assembly. The bypass switch is a single-pole double-throw circuit. The other six switches are single-pole single-throw designs. The lower isolation requirements of the input circuit compared to the filter switches allow a simpler single-throw element to be used.

For input levels between 3 and 10 watts, the attenuators are switched-out. For levels greater than 10 watts and less than 30 watts, the drive is routed through the 5 dB attenuator. For levels greater than 30 watts, the 9 dB attenuator is switched-in to limit the output to less than 12.6 watts. This attenuator system will allow the amplifier to operate over its full dynamic range without overdriving the driver amplifier input.

2.8.1.1 Attenuator

Figure 2.8.1.1-1 is a schematic of the diode switched attenuator. There are four possible RF paths through the switch:

1.	Bypass (Receive)	0 dB
2.	High Attenuation (Transmit)	9 dB
3.	Medium Attenuation (Transmit)	5 dB
4.	No Attenuation (Transmit)	0 dB

Simple series switched diodes are used to route the RF drive. Only one shunt diode is biased on in bypass mode to assure adequate isolation between input and output of the power amplifier gain stages. Sufficient isolation exists in the attenuation paths by reverse biasing the series diodes.

2.8.1.2 Overdrive Detector

A simple diode peak detector samples a portion of the RF drive at the output of the attenuator module through a resistive voltage divider (See Figure 2.8.1.1-1). The results of preliminary tests performed on the breadboard model are shown in Figure 2.8.1.2-1 and Table 2.8.1.2-1. Figure 2.8.1.2-1 is a graph of the drive level versus typical detected voltage. Table 2.8.1.2-1 lists the data compiled. The threshold for

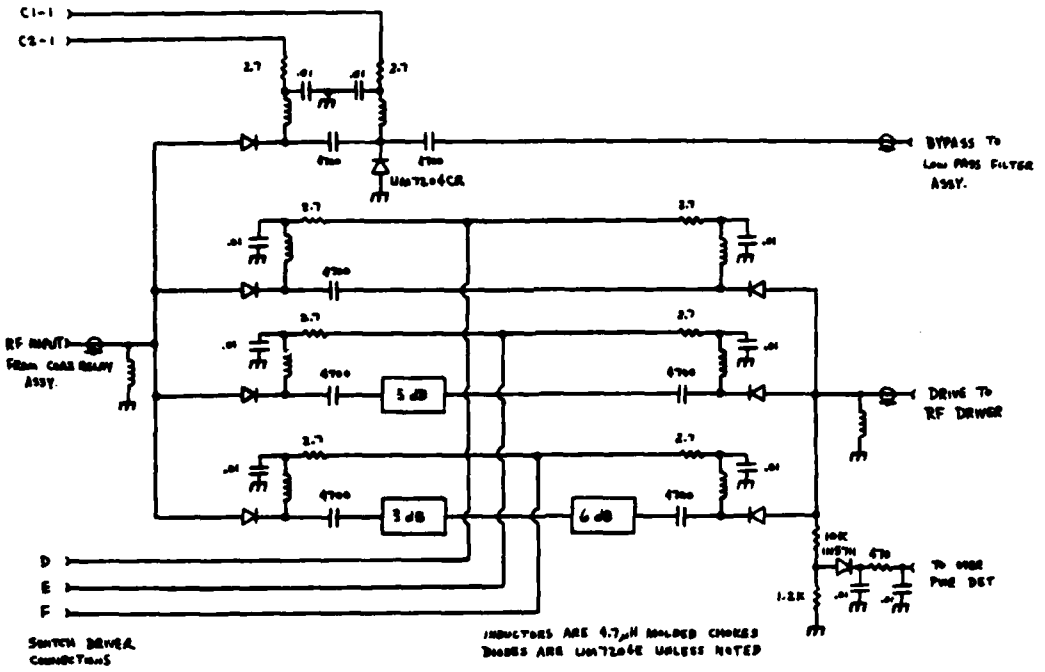


Figure 2.8.1.1-1 Attenuator And Detector Schematic

attenuator step-up will be 1.5 volts, or a corresponding input power level of 12 watts. This voltage is within the linear limits of the detector. A comparator shown schematically in Figure 2.8.1.2-2 will sense a voltage in excess of 1.5 volts and generate a negative-going TTL signal to initiate the attenuator step-up action.

Table 2.8.1.2-1 Detector Characteristics

Power In/Out (Watts)	Operating Frequency (MHz)			
	30	50	70	90
	Volts Detected			
5	0.90	0.90	0.90	0.90
8	1.23	1.25	1.25	1.25
10	1.40	1.40	1.45	1.45
30	2.60	2.70	2.75	2.80
50	3.70	3.80	3.80	3.90
80	4.80	4.90	5.00	5.10
100	5.40	5.40	5.40	5.70
Combined Loss of Switch and Detector (dB)				
	0.1	0.15	0.2	0.2

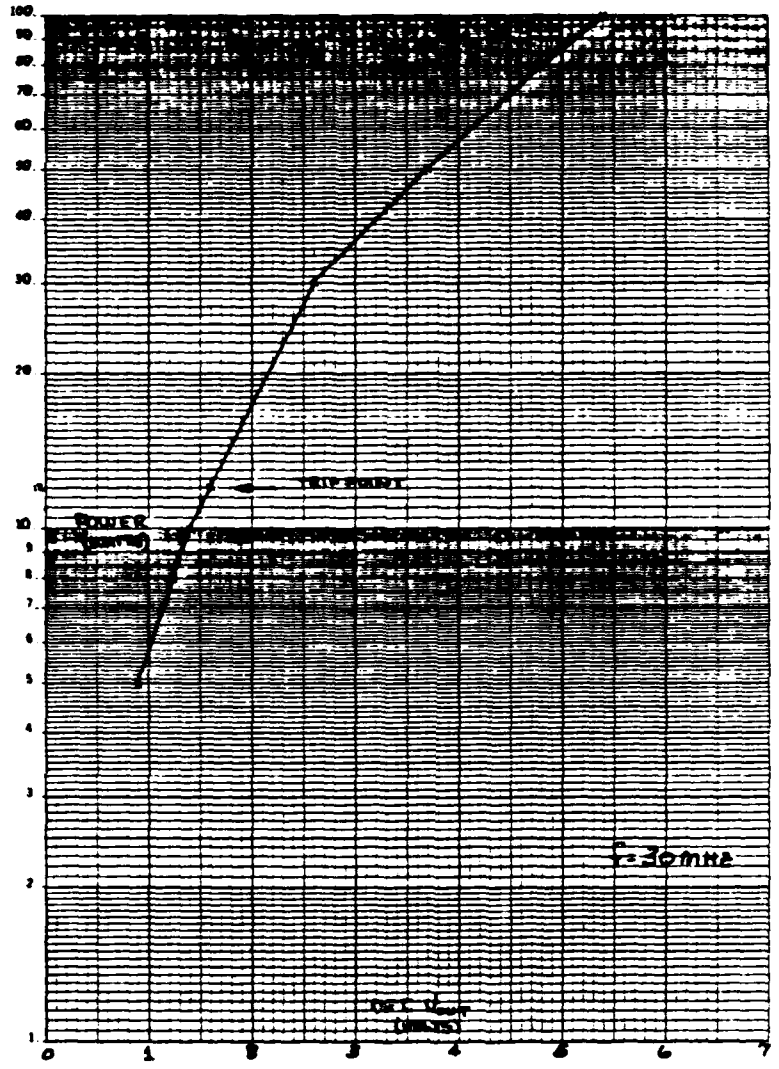


Figure 2.8.1.2-1 Drive Level Versus Detector Voltage

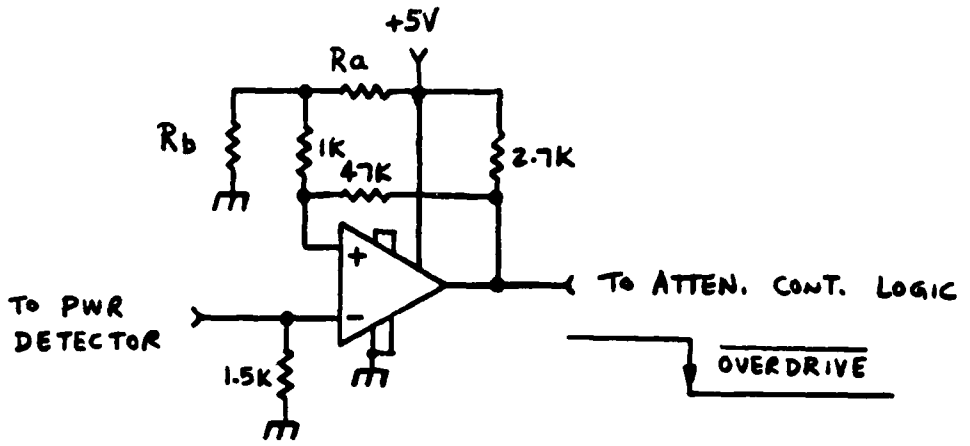


Figure 2.8.1.2-2 Overdrive Detector

2.8.1.3 Attenuator Control Logic

Figure 2.8.1.3-1 is the schematic of the logic that provides the interconnection between the control processor, the overdrive detector, and the switch drivers.

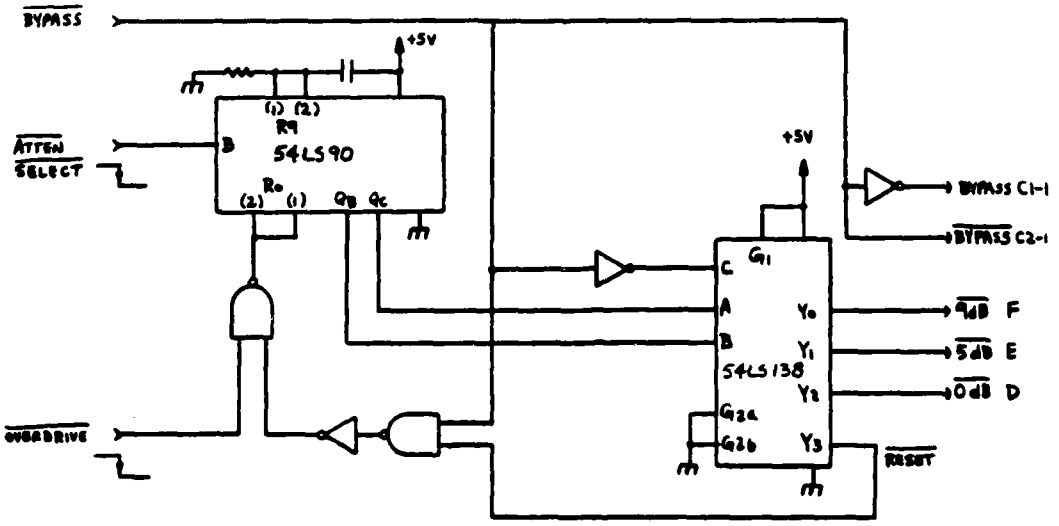


Figure 2.8.1.3-1 Attenuator Control Logic

U1 is a BCD counter connected bi-quinary that powers-up preset to count nine. Subsequent negative-going "Attenuator Select" commands from the control processor will step the counter to all zeros and then begin a binary count. The 2^1 and 2^2 output from the counter and bypass command from the control processor are decoded by the 3- to 8-line decoder (U2). Its output drives the individual switch drivers. The state diagram shown in Figure 2.8.1.3-2 describes the sequential functioning of the attenuator control logic. The amplifier may power-up with the logic in either transmit mode (commanding 9 dB of attenuation) or receive mode (bypass). In the transmit case, the first step change from the controller will not effect an attenuation reduction. Subsequent step commands from the controller will advance the attenuator from 9 dB to 5 dB to no attenuation and then back to 9 dB attenuation. If the amplifier powers-up in the bypass mode, the condition will be transient and the input attenuator would immediately switch to the 9 dB attenuator or bypass depending on commands from the system controller. Note that the coaxial mechanical relays (A3) on the amplifier input and output will stay in the bypass condition until the system controller has completed its power-up sequence. The attenuator will then be set to 9 dB and power leveling would begin upon initiation of drive.

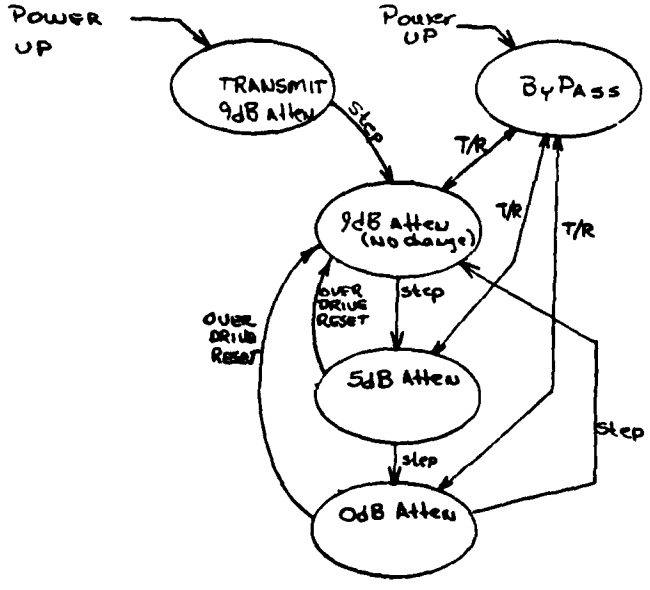


Figure 2.8.1.3-2 Attenuator Control State Chart

2.8.1.4 Switch Drivers

The switch drivers used to drive the PIN diodes in the attenuator are very similar to the designs discussed in paragraph 2.7.1.2 of this report. The only difference is the lower power handling requirement (100 watts maximum) permitting biasing the PIN diodes at a lower current level (0.2 amps versus 0.5 amps per diode in the output circuit). The lower current requirement eliminates the need for a high gain darlington drive circuit to assure saturation of the negative bias switching transistor. Figure 2.8.1.4-1 is a schematic of a switch driver circuit.

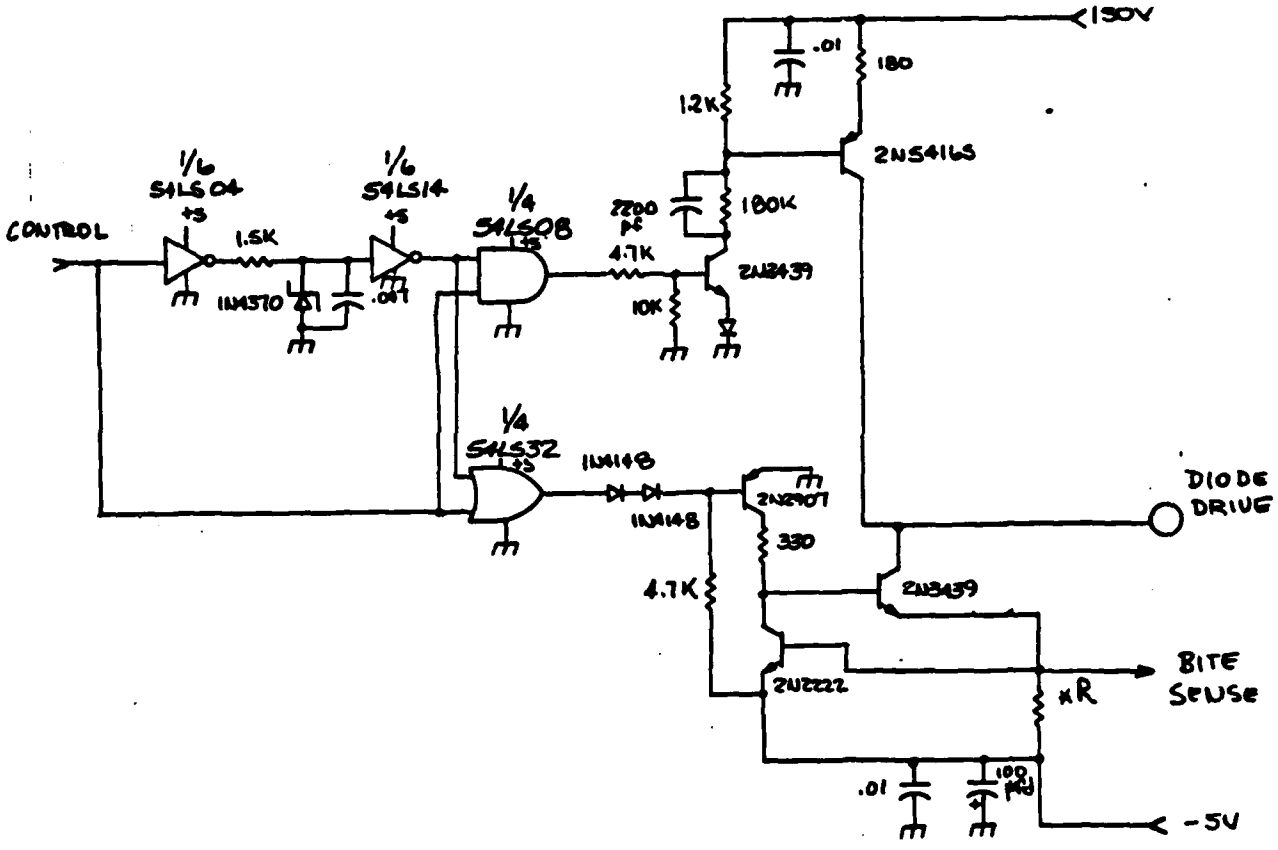


Figure 2.8.1.4-1 Attenuator Switch Driver

2.8.1.5 BITE

Active BITE monitoring is identical to that used in the harmonic filter switch driver circuit (Section 2.7.1.2). The currents in the driver stages and the +150 and -5-volt supplies are constantly monitored by comparator circuits. The outputs of the comparators are periodically interrogated by the system controller to examine module status.

2.8.2 Frequency Counter And Drive Detector Circuits

The schematic diagram of the frequency counter, drive detector and the amplifiers for driving them is shown in Figure 2.8.2-1. These circuits are described in this section.

The input amplifier consists of two 2N918 transistors connected in a cascode configuration with input and output frequency shaping networks. The cascode configuration minimizes reverse power gain allowing stable operation at higher forward power gains. This amplifier is stable with any load or source termination as long as the 470-ohm collector load resistance is in place. Plots of gain and compression characteristics are shown in Figures 2.8.2-2 and 2.8.2-3, respectively.

The input amplifier is driven from a divider which samples the RF signal. The forward attenuation in the divider is approximately 50 dB, while the reverse attenuation is 53.6 dB. This ensures that the spurious levels at the input side of the divider will be less than -103.6 dBc.

The input amplifier drives the detector and a pad which in turn drives the counter amplifier. The pad masks the changes in input impedance of the counter amplifier as frequency and power level change. This preserves the gain flatness of the input buffer so that the detector trip level is relatively consistent across the band.

The configuration and operation of the amplifier which drives the counter are identical to those of the input amplifier. Some component values in the frequency shaping networks are different due to the fact that the load is different. The counter amplifier also acts as a limiter so that the counter is not over driven at the higher RF drive levels.

The drive detector consists of a comparator, a peak detector, and a temperature compensation network. The peak detector output is compared to a reference voltage which tracks the peak detector bias over temperature. If the peak detector output is higher than the reference, the comparator output is low, signalling the presence of an RF carrier. Otherwise, the comparator output is high. The offset adjustment can be set so that the comparator inputs are near the threshold when no RF is applied, or it can be set to trip the comparator at a specified RF input level. Sufficient gain is provided in the input amplifier to ensure that the drive detector trip level can be set below +26 dBm in any production unit.

The drive detector response times are shown in Figure 2.8.2-4. This data shows that the drive detector can indicate the absence or presence of an RF input within 0.5 microseconds after the corresponding event. The data was taken with a +25 dBm RF signal; the response times improved slightly as the RF power was increased.

The counter circuitry consists of two cascaded four-bit asynchronous binary counters, an eight-bit latch, and a 2N2222A transistor. The

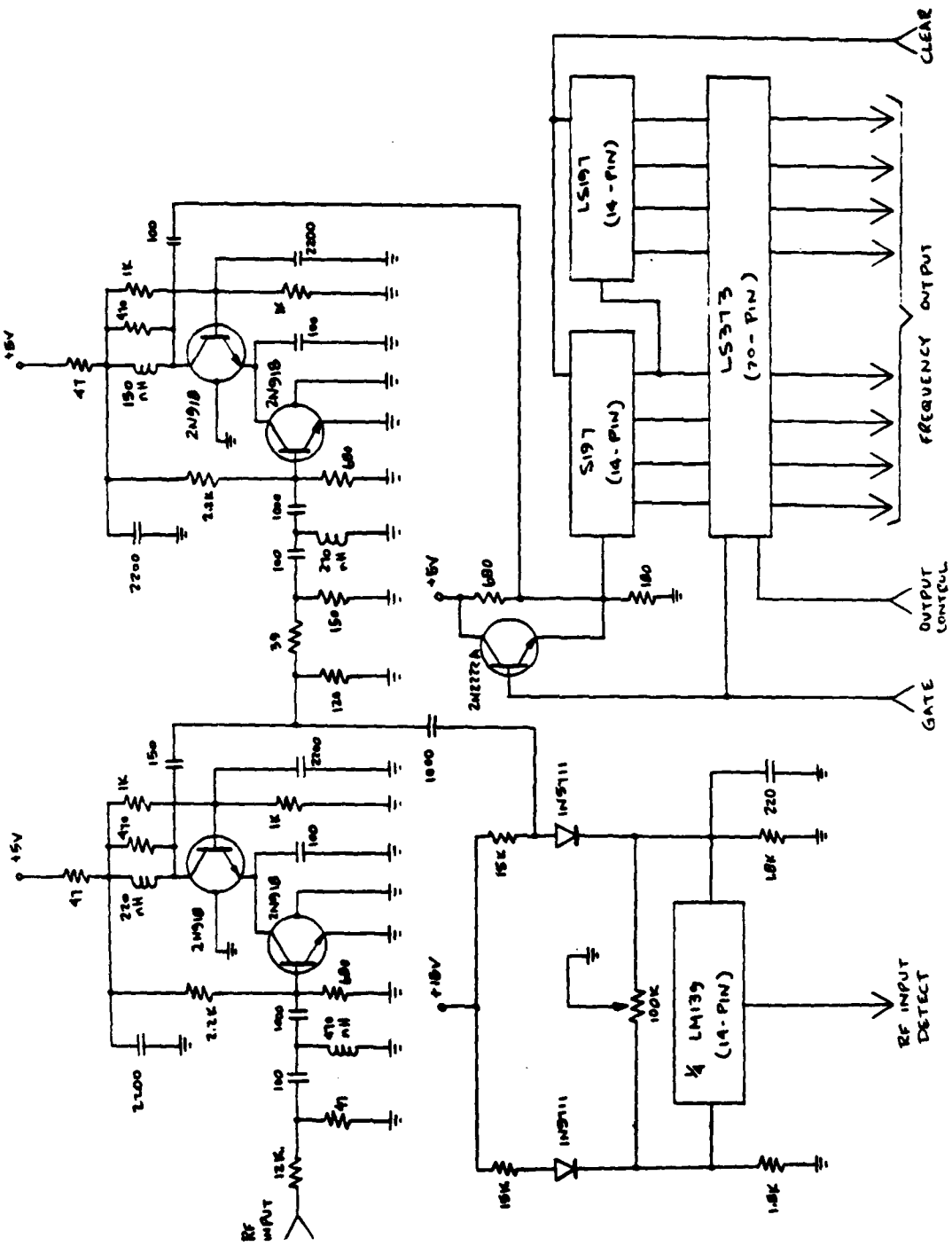


Figure 2.8.2-1 Frequency Counter, Drive Detector, And Input Amplifier Schematic

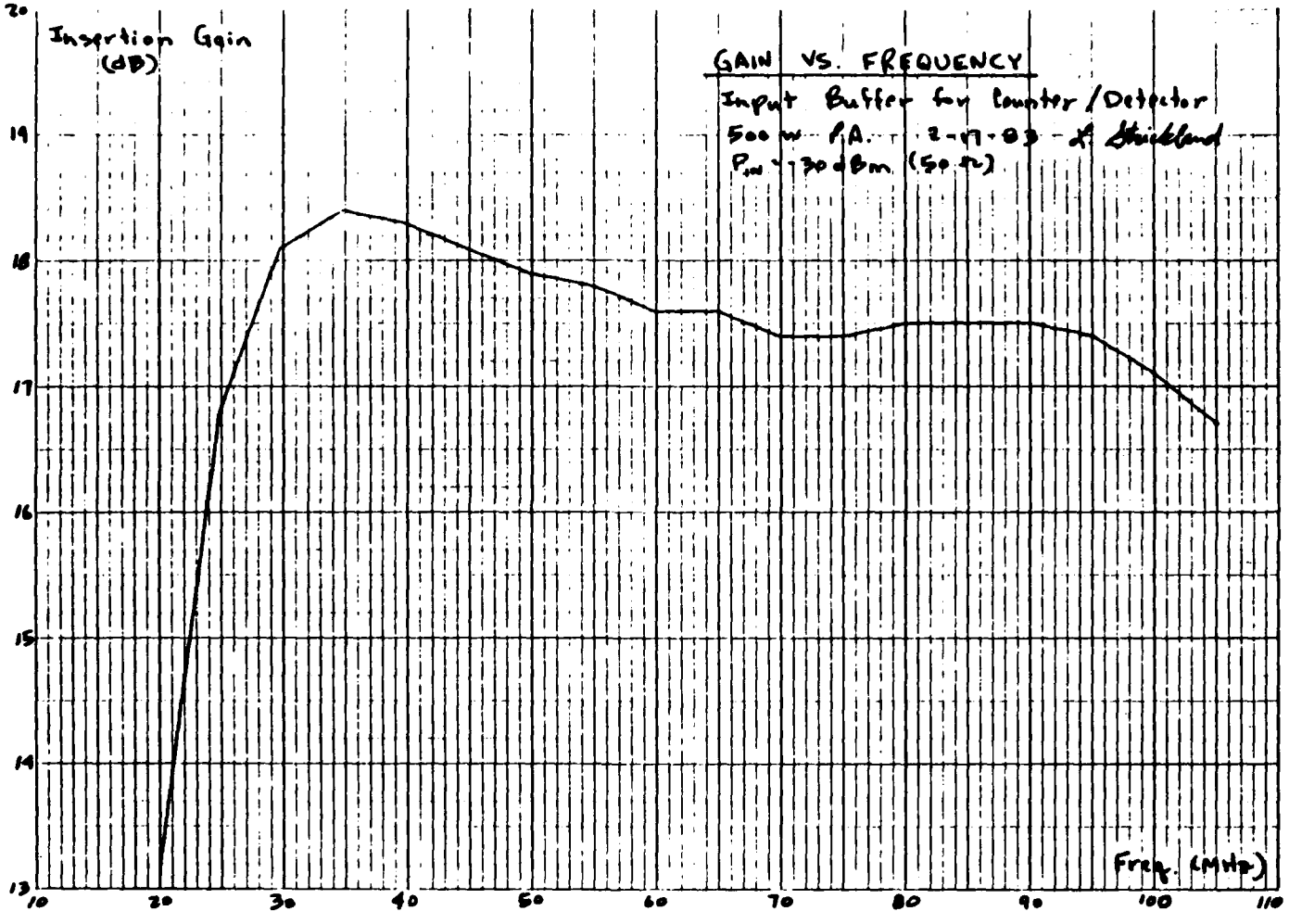


Figure 2.8.2-2 Input Amplifier Gain Versus Frequency

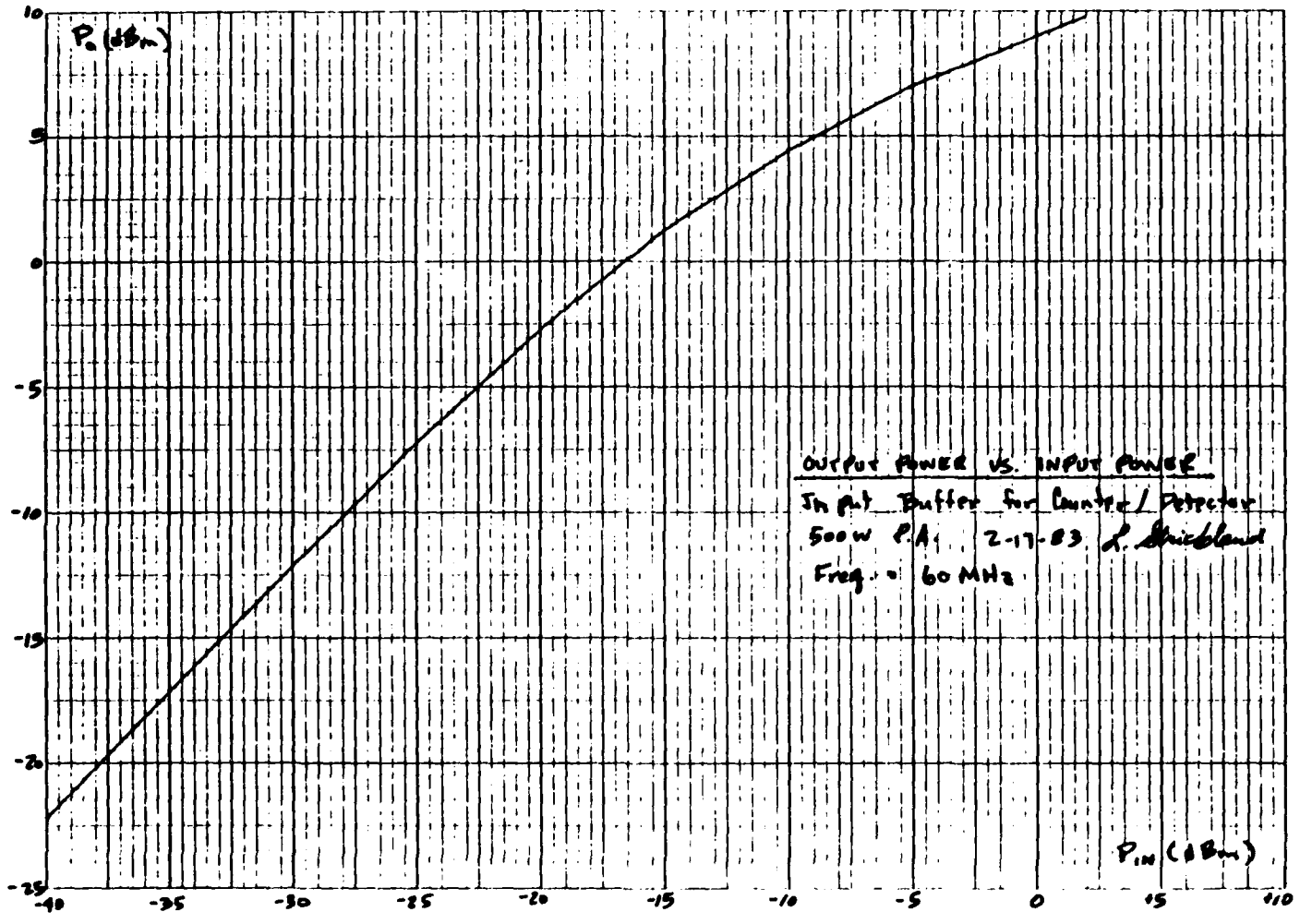
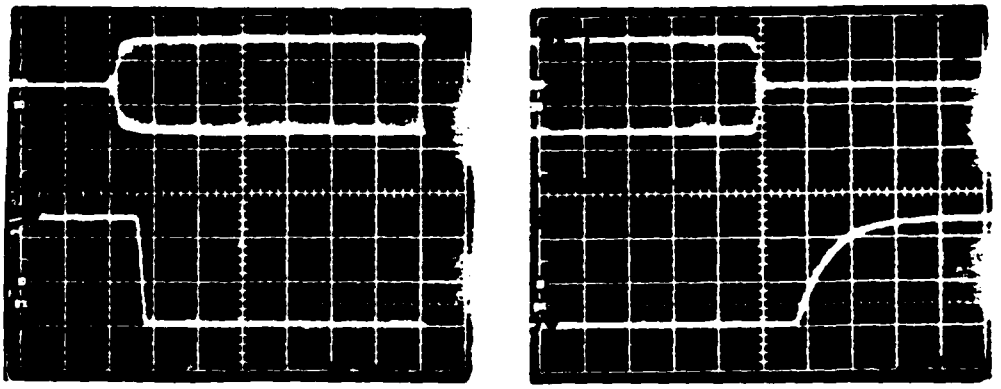


Figure 2.8.2-3 Input Amplifier Output Power Versus Input Power



0.5 Microseconds per horizontal division

Figure 2.8.2-4 Drive Detector Response Times

counter functions as follows. First, the clear input is driven low to set all counter outputs to zero. Then the clear input goes high, allowing the counters to count the negative transistions coming from the counter amplifier. Next, the gate pulse goes high, which does two things:

(1) The 2N2222A transistor is turned on and holds the input to the counter high so that it stops counting, and
(2) The LS373 latches to the last count on the counter outputs. The gate pulse then goes low so that the latch holds the count and the clear pulse again goes low so that the counters are reset and the cycle begins again.

The timing diagram for the counter is shown in Figure 2.8.2-5

From the timing diagram one can see that the update period is 2 microseconds and the count time is 1.5 microseconds. This yields a frequency resolution of 667 kHz.

The minimum drive levels into the counter which produce a proper count are shown in Table 2.8.2-1. Sufficient gain is provided by the input amplifier and counter amplifier to ensure that the counter will count any RF signal larger than +30 dBm, worst case. The counter amplifier output is limited to approximately 1.5 V p-p, preventing improper counting at high drive levels.

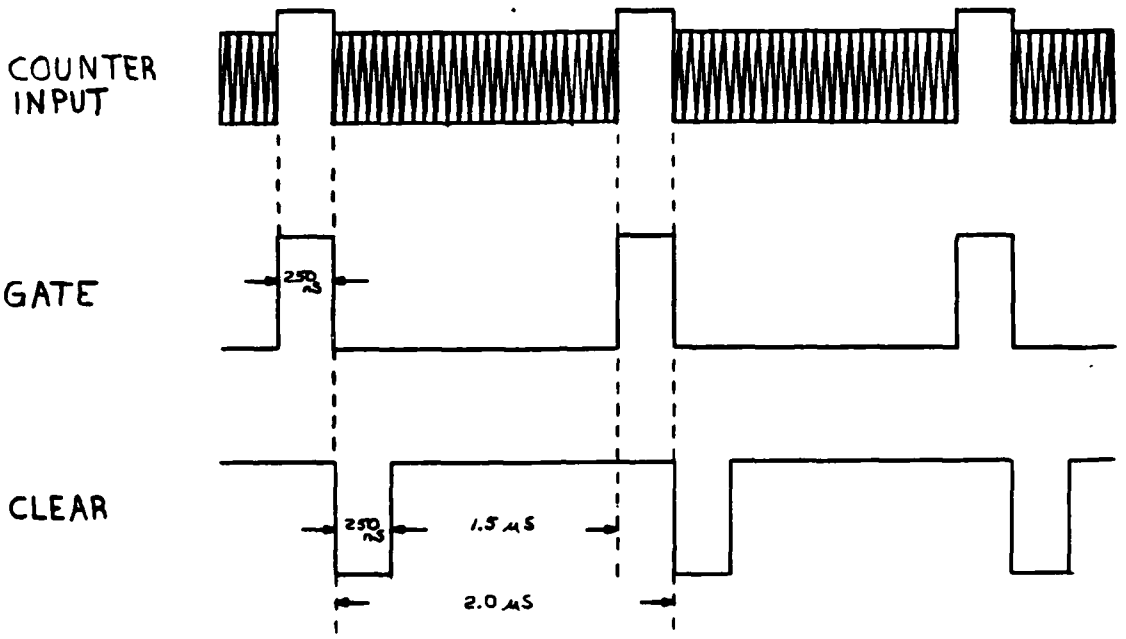


Figure 2.8.2-5 Frequency Counter Timing Diagram

Two problems present in the initial design have been corrected during the breadboard test effort. First, the frequency resolution was discovered to be worse than 667 kHz because the gating transistor (2N2222A) was used to switch off the bias to the last 2N918 in the counter amplifier. This design caused an extra negative transition at the output of the counter amplifier that was sometimes picked up by the counter. The problem was resolved by putting the gating transistor in its present location where it holds the input of the counter high during the hold sequence. Since no bias is changed in the counter amplifier, there are now no extra negative transitions. The second problem was that at the low end of the band and at high drive levels, the counter used to respond to second harmonic generated in the counter amplifier. This problem was resolved by changing the frequency shaping network in the output of the counter amplifier so that it does not transform the counter input impedance up to such a high value at the low end of the band.

Table 2.8.2-1 Frequency Counter Test Data

FREQUENCY (MHZ)	MINIMUM POWER REQUIRED FOR DETECTOR OUTPUT = 0.10 VDC (dBm)	MINIMUM POWER REQUIRED FOR COUNTER TO COUNT (dBM)
30	19.6	16.2
35	17.5	14.4
40	17.4	14.8
45	16.6	16.6
50	16.5	16.8
55	16.6	16.7
60	16.8	16.4
65	16.8	16.8
70	16.9	16.9
75	17.0	17.2
80	17.8	18.4
85	18.6	18.8
88	18.9	19.5
90	15.7	19.9

INPUT FREQUENCY (MHz)	LATCH OUTPUT	FREQUENCY INDICATED (MHz)
30	0 0 1 0 1 1 0 1	30.000
40	0 0 1 1 1 1 0 0	40.000
	0 0 1 1 1 1 0 1	40.667
50	0 1 0 0 1 0 1 1	50.000
	0 1 0 0 1 1 0 0	50.667
60	0 1 0 1 1 0 1 0	60.000
	0 1 0 1 1 0 1 1	60.667
70	0 1 1 0 1 0 0 1	70.000
	0 1 1 0 1 0 1 0	70.667
80	0 1 1 1 1 0 0 0	80.000
	0 1 1 1 1 0 0 1	80.667
90	1 0 0 0 0 1 1 1	90.000
	1 0 0 0 1 0 0 0	90.667

2.9 SIX-WAY SPLITTER (A8)

The six-way RF power splitter is a passive device that divides the output of the RF driver amplifier into six equal parts to uniformly drive the six paralleled RF output amplifiers. The splitter is matched to the combiner (A9) such that the driver amplifier power is split and summed in amplitude and phase to minimize RF losses. In addition, isolation between output ports is provided to minimize interaction between amplifiers (to avoid potential feedback conditions) and to reduce the input VSWR in the event of an output RF amplifier failure. Balance between outputs ensures equal sharing of the output load between amplifiers.

The six-way RF power splitter consists of a balun, a 4:1 impedance transformer, and a six-way splitter that parallels the six 50-ohm output loads. In the ideal case, this combination would present a 1.5:1 VSWR to the driving source. However, the three basic components of the splitter all exhibit some series parasitic inductance because of the physical interconnection paths. This characteristic is used to the advantage of the splitter, because three strategically placed shunt capacitors interact with the series inductance to form a three-section L-network with an impedance transformation of 1.5:1. The overall impedance transformation of the six-way splitter is 6:1, as needed. Figure 2.9-1 is the equivalent circuit of the six-way RF power splitter.

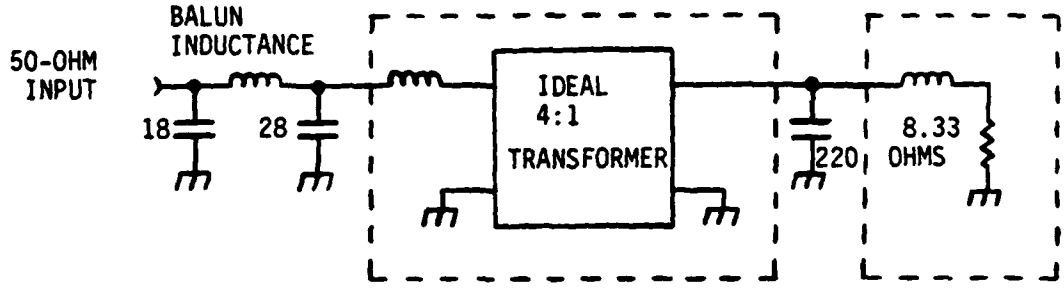


Figure 2.9-1 Six-Way RF Power Splitter Equivalent Circuit

2.9.1 Construction

The six-way RF power splitter utilizes nine ferrite-loaded transmission line sections: one for the balun, two for the 4:1 transformer, and six for the splitter. Ferrite loading of the lines reduces common-mode currents that tend to short out the splitter. For even power distribution to the six output ports, the six splitter lines are arranged in a center-fed hexagon configuration. The six splitter lines are composed of 0.250-inch diameter 50-ohm semirigid coax lengths, each loaded with three Fair-Rite 5965001901 ferrite cores with an initial permeability of 100. The two 4:1 transformer lines are also 0.250-inch

diameter coax, but are loaded with three 5967001901 cores with an initial permeability of 40. The balun consists of two turns of 50-ohm flexible coax through two 5967001901 cores. Six ATC-100B series ceramic chip capacitors improve the overall broadband impedance match of the splitter to better than 1.3:1 VSWR from 30 to 88 MHz. Figure 2.9.1-1 is a schematic diagram of the six-way RF power splitter. Port-to-port isolation is provided by a star arrangement of six 35-ohm 20-watt thin film RF power resistors. Figure 2.9.1-2 is a photograph showing the physical layout of the breadboard splitter.

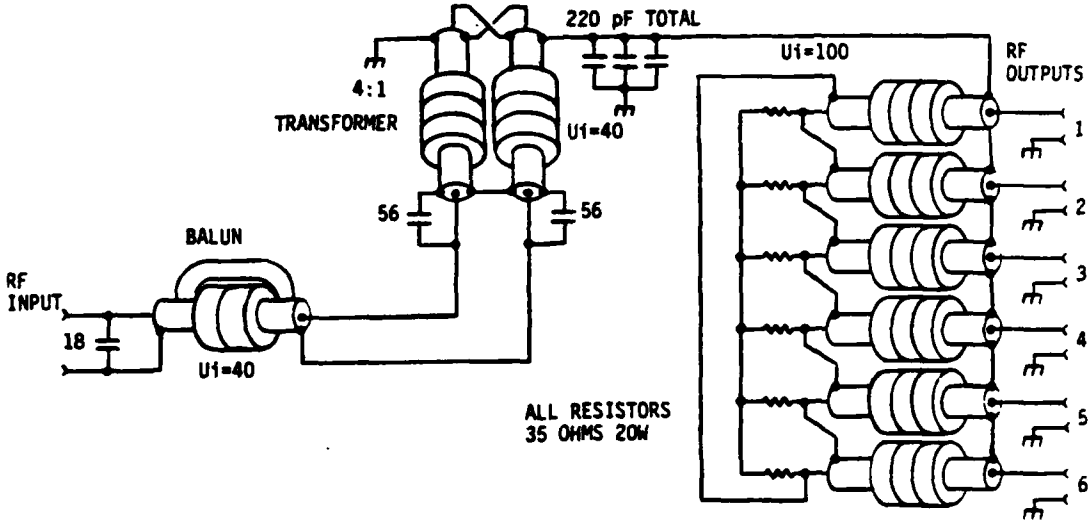


Figure 2.9.1-1 Six-Way RF Power Splitter Schematic

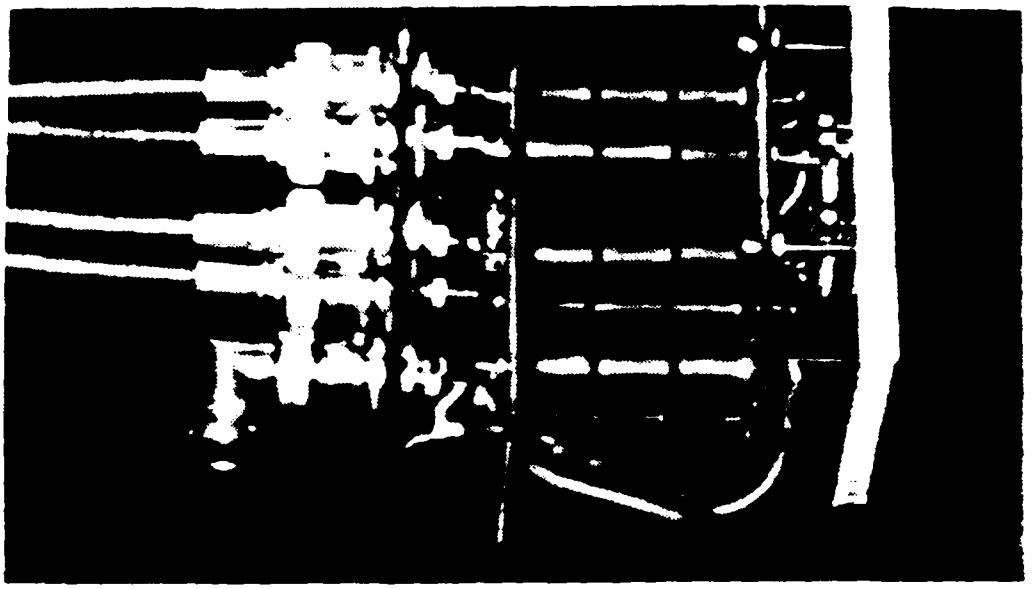


Figure 2.9.1-2 Breadboard Six-Way Power Splitter

2.9.2 Performance

The important performance parameters of the six-way RF power splitter are input VSWR, isolation, and insertion loss. Tables 2.9.2-1 through 2.9.2-3 list the respective measured performance data of the breadboard six-way RF power splitter. Because of the six-way power division, the ideal loss to each port is 7.78 dB. Total loss is calculated by converting the individual port dB numbers to power fractions, adding the fractions, and converting back to dB.

Table 2.9.2-1 Input VSWR

	FREQUENCY (MHz)						
	30	40	50	60	70	80	90
RETURN LOSS (dB)	18.0	27.3	28.8	20.7	19.0	21.9	30.0
VSWR	1.28	1.10	1.08	1.20	1.25	1.18	1.08

Table 2.9.2-2 Port-To-Port Isolation (dB)

	FREQUENCY (MHz)						
PORT 1 TO:	30	40	50	60	70	80	90
PORT 2	16.7	16.3	16.1	16.2	16.4	16.6	16.4
PORT 3	19.5	20.6	21.6	22.0	21.6	20.9	20.5
PORT 4	16.7	17.5	18.1	18.4	18.2	17.7	17.4
PORT 5	19.7	19.9	22.0	22.5	22.2	21.6	21.2
PORT 6	17.0	17.5	16.3	16.3	16.5	16.7	16.4

Table 2.9.2-3 Insertion Loss (dB)

	FREQUENCY (MHz)						
INPUT TO:	30	40	50	60	70	80	90
PORT 1	8.13	8.07	8.09	8.13	8.16	8.18	8.19
PORT 2	8.12	8.06	8.07	8.12	8.14	8.14	8.13
PORT 3	8.10	8.02	8.01	8.02	8.02	7.98	7.92
PORT 4	8.10	8.02	8.01	8.03	8.03	7.98	7.94
PORT 5	8.11	8.05	8.05	8.08	8.09	8.07	8.04
PORT 6	8.12	8.05	8.07	8.12	8.16	8.16	8.16
TOTAL LOSS	.33	.26	.27	.30	.32	.30	.28

2.10 SIX-WAY COMBINER (A9)

The six-way RF power combiner is a passive device used to sum the outputs of the six RF power output amplifiers to a common 50-ohm output line. The combiner is essentially a mirror image to the power splitter, but is designed to handle much higher power levels. Because of the output power required from this module, significant effort is necessary to minimize losses and guarantee adequate voltage breakdown capability.

2.10.1 Construction

The six-way RF power combiner utilizes nine ferrite-loaded transmission line sections, as does the six-way RF power splitter. The six 50-ohm combiner lines are composed of concentric brass tubes aligned by machined Teflon spacers and loaded with four Fair-Rite 5967000501 ferrite cores with an initial permeability of 40. Also constructed from brass tubes, the two 25-ohm 4:1 transformer lines are each loaded with seven 596700501 cores, as is the 50-ohm balun. Figure 2.10.1-1 is a photograph of the breadboard 500-watt VHF power amplifier showing the relative sizes of the six-way RF power combiner and splitter. Figure 2.10.1-2 is the electrial schematic of the combiner.

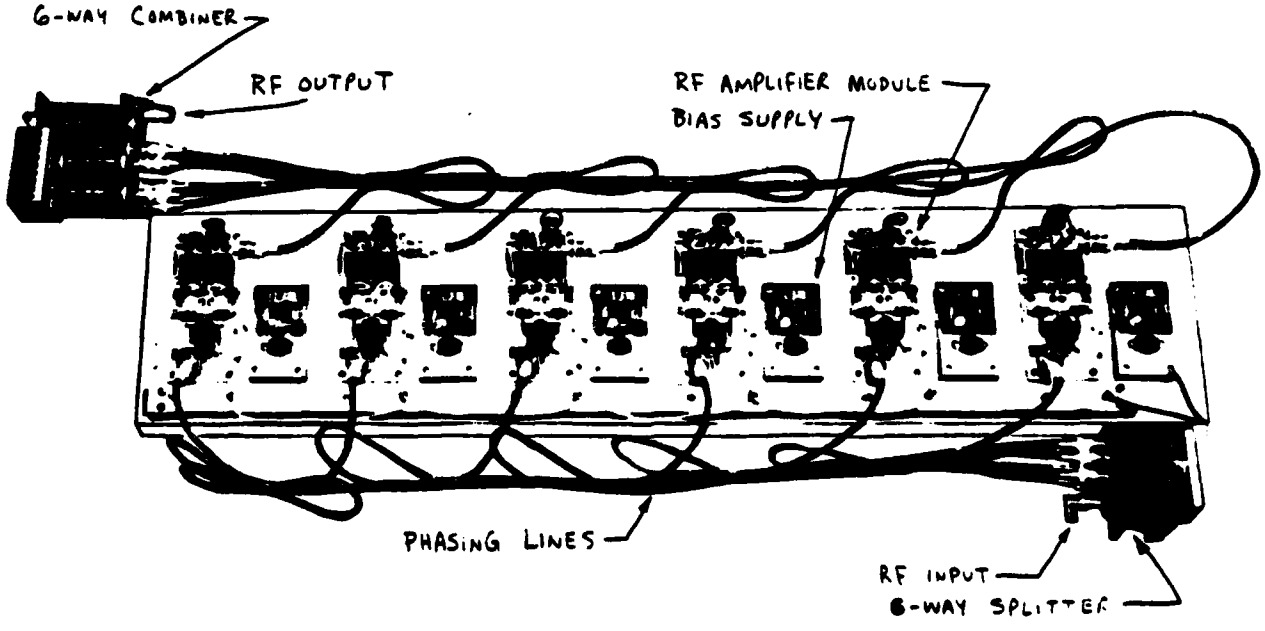


Figure 2.10.1-1 Breadboard 500-Watt Power Amplifier

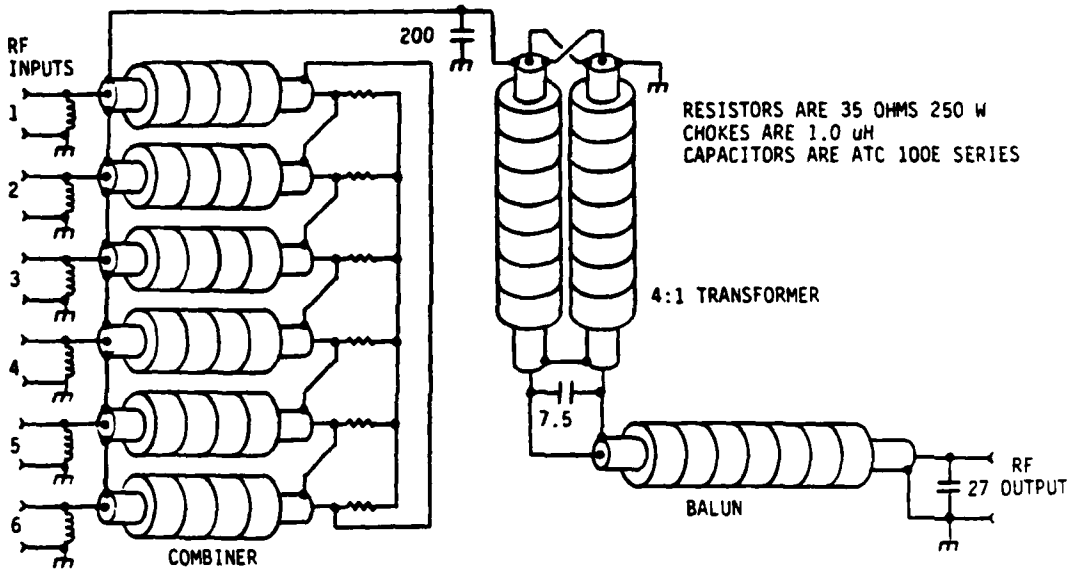


Figure 2.10.1-2 RF Power Combiner Schematic

2.10.2 Performance

Performance data for the six-way RF power combiner is listed in Tables 2.10.2-1, 2.10.2-2, and 2.10.2-3. The low pass L-matching networks inherent in the combiner equivalent circuit assist the low pass filter assembly (A6) in rejecting above-band emissions. Figure 2.10.2-1 is a computer-generated graph of the measured broadband response of the RF power combiner showing its contribution to the overall harmonic rejection of the 500-watt VHF power amplifier.

Table 2.10.2-1 Input VSWR

	FREQUENCY (MHz)						
	30	40	50	60	70	80	90
RETURN LOSS (dB)	16.5	19.4	20.2	18.2	16.0	14.5	13.5
VSWR	1.35	1.24	1.22	1.28	1.38	1.40	1.54

Table 2.10.2-2 Port-To-Port Isolation (dB)

	FREQUENCY (MHz)						
PORT 1 TO:	30	40	50	60	70	80	90
PORT 2	15.7	15.6	15.5	15.4	15.3	15.1	15.0
PORT 3	22.9	24.2	25.0	25.0	25.0	25.0	25.0
PORT 4	18.3	18.5	19.0	19.1	19.4	19.8	20.1
PORT 5	20.3	21.1	22.0	23.0	24.0	24.9	25.0
PORT 6	16.4	16.1	15.7	15.3	15.0	14.7	14.5

Table 2.10.2-3 Insertion Loss (dB)

	FREQUENCY (MHz)						
OUTPUT TO:	30	40	50	60	70	80	90
PORT 1	8.09	8.00	8.01	8.06	8.12	8.23	8.33
PORT 2	8.08	8.00	8.00	8.00	8.05	8.14	8.20
PORT 3	8.09	8.00	8.01	8.04	8.11	8.20	8.34
PORT 4	8.09	8.01	8.01	8.04	8.13	8.24	8.40
PORT 5	8.11	8.02	8.01	8.06	8.14	8.27	8.40
PORT 6	8.11	8.03	8.02	8.06	8.16	8.30	8.44
TOTAL LOSS	.31	.23	.23	.26	.34	.45	.55

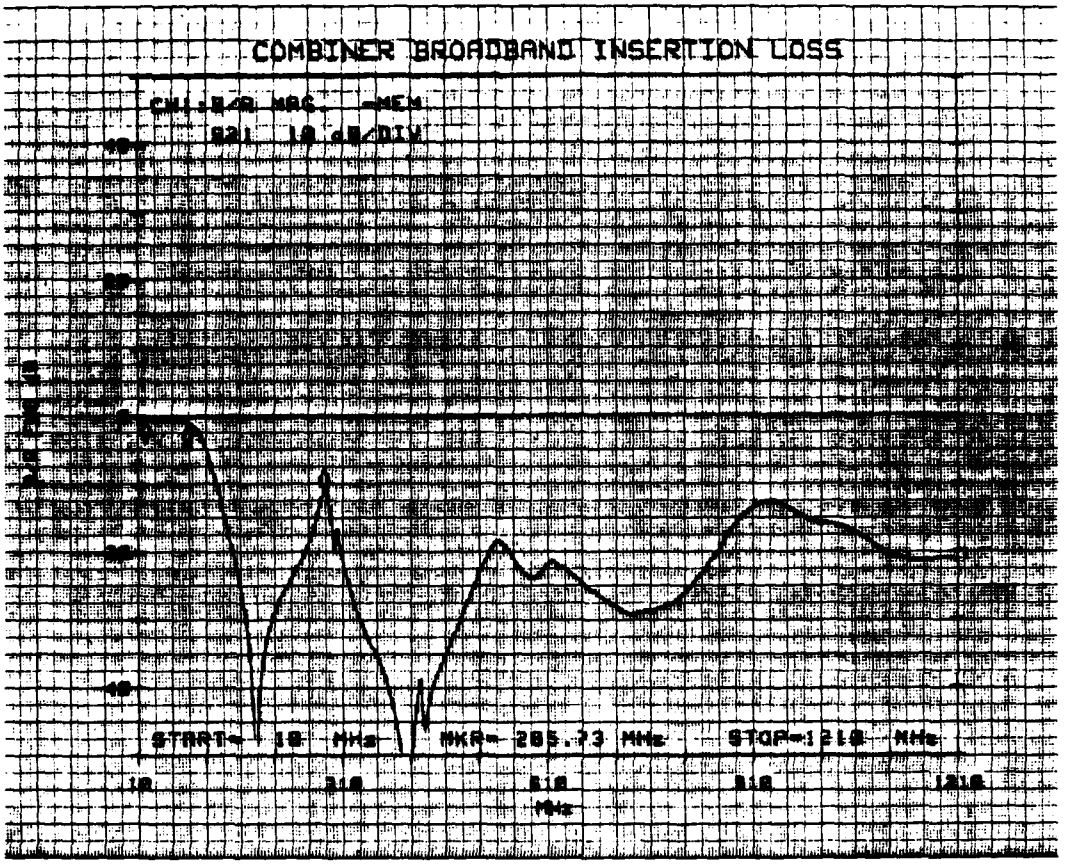


Figure 2.10.2-1 Six-Way RF Power Combiner Broadband Response

2.11 DRIVER AMPLIFIER POWER SUPPLY (A10)

The driver amplifier power supply is a switching regulator to provide a primary power voltage of 28 volts to the companion RF driver amplifier (A11) and isolate the amplifier from the vehicular supply. The switching converter is synchronized to an external clock and operated out-of-phase with the control circuit power supply to reduce conducted switching emissions. The power supply also shares part of the input EMI filter and loop-damping filter with the control circuit power supply to conserve space. The supply is identical to the RF output amplifier power supply with the exception that the 4-volt secondary output is not used.

Section 2.6 of this report contains detailed technical information concerning the design of the driver amplifier power supply.

2.12 RF DRIVER AMPLIFIER ASSEMBLY (A11)

The RF driver amplifier assembly amplifies the attenuated RF input signal to a level sufficient to drive the six combined RF output amplifiers. The six-way RF power splitter loaded with the six RF output amplifiers presents a high load VSWR to the RF driver amplifier. The driver amplifier is designed to safely deliver its rated output power into this high VSWR without oscillating or generating spurious noise or sidebands. The amplifier and corresponding power supply are separated because of packaging volume constraints. Although a separate variable attenuator was proposed for RF power level control, this function has been incorporated in the driver amplifier by using variable-gain push-pull power-MOSFET devices. The result is a stable, rugged, high-gain amplifier with very-high-speed ALC capability. Table 2.12-1 lists the power output and load VSWR requirements of the driver amplifier. The power input to the driver amplifier may vary from 2.5 to 12 watts.

Table 2.12-1 Driver Amplifier Power Output Requirements

	FREQUENCY (MHZ)						
	30	40	50	60	70	80	88
P_{out} (W)	15	25	40	45	60	60	75
LOAD VSWR	6:1	5:1	4:1	3:1	2:1	2:1	1:1

Originally, the RF driver amplifier was to be a scaled-down version of the bipolar output amplifiers, following a variable power-attenuator for RF power level control. A breadboard bipolar driver amplifier was abandoned before becoming fully functional because of obstacles encountered in developing a variable power-attenuator. Several attenuator circuits performed well during low-power evaluation testing, but all units failed to meet the power handling requirements of the 500-watt VHF power amplifier. Figure 2.12-1 illustrates the attenuator circuits evaluated, and lists advantages and disadvantages. A combination PIN diode/MOSFET attenuator formed by cascading the circuits of Figure 2.12-1 (A) and (C) was evaluated and offered wide bandwidth for small corrections, wide dynamic range, and a lead-lag frequency response, but the circuit was large and complex, and the RF rectification problems in the PIN diodes could not be solved.

Considerable research and contacts with Motorola, CTC, Acrian, and Siliconix representatives led to the consideration of a variable-gain power-MOSFET driver amplifier. The initial concern was whether or not full output could be obtained with the FETs biased for very low gain, because all published AGC curves showed constant input power with gate bias adjustment to control the output power. A push-pull MOSFET amplifier was constructed using a pair of available CTC BF50-35 50-watt parts. As hoped, the saturated RF output power changed very little with

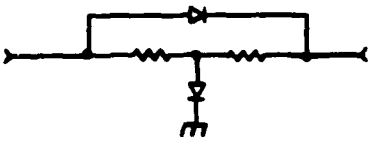
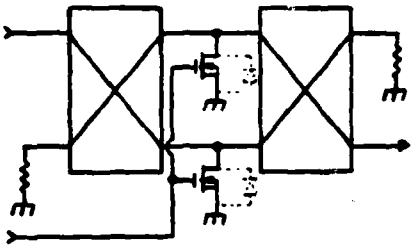
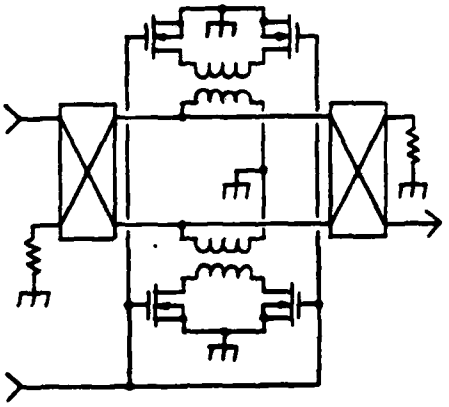
CIRCUIT CONFIGURATION	ADVANTAGES	DISADVANTAGES
 (A) Bridged-TEE PIN Diode Attenuator	• 25 dB Dynamic Range • Constant Input Impedance • Simple, Compact Circuit • Only 0.8 dB Loss	• 10 kHz Bandwidth Due To Slow Diodes • Discontinuous Control Function At High Power Due To Diode Rectification
 (B) Power MOSFET Attenuator	• Wide Bandwidth	• 4 dB Loss And 12 dB Dynamic Range Because Of Compromise Between MOSFET Capacitance And ON Resistance • Stops Working At Relatively Low Power Level Because Of Rectification In Parasitic Diode In MOSFET
 (C) Push-Pull Power MOSFET Attenuator	• Wide Bandwidth • Handles Power Level Comparable To PIN Diode Attenuator	• Only 7 dB Dynamic Range • FETs Latch ON At 12.5 Watts At Low End Of Band Due To Carrier Lifetime Of Parasitic Diodes

Figure 2.12-1 Attenuator Circuits Evaluated

bias adjustment. The next concern was damage to the MOSFET gate in the event of accidental overdrive of the power amplifier. The Motorola and CTC devices have a rated gate-to-source breakdown voltage of +/-25 VDC, but the Acrian and Siliconix devices are rated at +/- 40 VDC and are tested at +/- 50 VDC. Motorola was eliminated from consideration and CTC was acquired by Acrian. Figure 2.12-2 is a schematic of the BF50-35 amplifier.

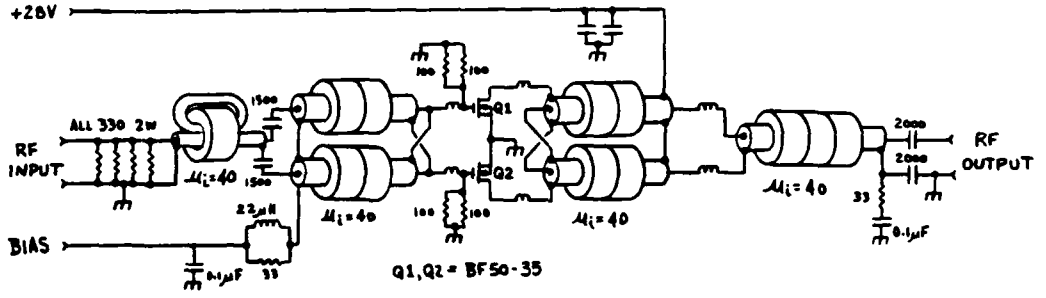
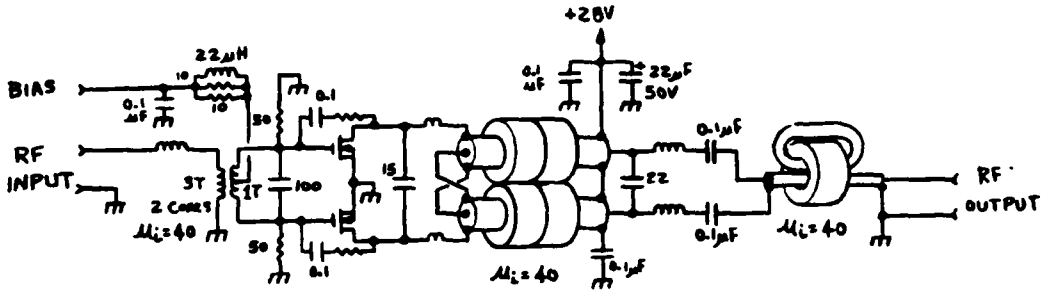


Figure 2.12-2 Breadboard CTC BF50-35 Power MOSFET Amplifier Schematic

Further testing with the breadboard BF50-35 amplifier revealed a necessary compromise in designing MOSFET power amplifiers. Because the input impedance of the MOSFET is primarily capacitive, resistive loading is required to obtain a low broadband input VSWR, but power gain is sacrificed. It was decided to design the amplifier for maximum stable gain, and then quadrature-combine a pair of amplifiers to maintain a low input VSWR. With size, availability, gate breakdown voltage, and output power at high VSWR as considerations, the Siliconix DV2880V push-pull 80-watt power MOSFET was chosen. Acrian is developing a similar device.

Because of the excess power output capability of a pair of 80-watt devices and the limited space in the RF driver amplifier module, 54 to 88 MHz quadrature hybrid power combiners were chosen. The power imbalance of approximately 3 dB at 30 MHz does not limit the application of the amplifier. The Anaren 1A0230-3 chosen measures 2.10x2.00 inches.

Next, an evaluation amplifier was constructed using a DV2880V. The amplifier was optimized empirically in a high-power swept test position. Feedback was added to suppress an oscillation. Figure 2.12-3 is a schematic of the amplifier, with 40-watt test data listed. Performance of the amplifier was inadequate, but the circuit offered a data base from which a more sophisticated amplifier could be designed.



	FREQUENCY (MHz)						
	30	40	50	60	70	80	90
P_{IN} (W)	5.20	2.68	2.00	1.52	1.29	1.20	1.53
P_{REF} (W)	4.00	1.82	1.15	0.68	0.39	0.29	0.48
I_D (A)	4.1	3.6	3.6	3.5	3.6	3.6	3.8
Gain (dB)	8.9	11.7	13.0	14.2	14.9	15.2	14.2
Efficiency (%)	35	40	40	41	40	40	38
Return Loss (dB)	1.1	1.7	2.4	3.5	5.2	6.2	5.0

NOTE: Test Conditions Output Power = 40 Watts
Quiescent
Drain Current = 2 Amps

Figure 2.12-3 Transformer-Matched DV2880V Amplifier Schematic And Data

A single-ended amplifier designed to deliver 20 watts to a 25-ohm load was used to model one-half of the desired 40 watt, 50-ohm output network. With 60 percent DC to RF conversion efficiency as a goal, the peak voltage swing at the drain was assumed to be .60 x 28V = 21.7V.

Therefore, Rout = (21.7x21.7)/(2x20) or about 12 ohms.

A conventional two-section L-network was designed to match 12 ohms to 25 ohms using a low pass section at 90 MHz followed by a high-pass section at 30 MHz. Figure 2.12-4 is a schematic of the amplifier model showing starting values for the matching network components. Figure 2.12-5 is a listing of the SUPER-COMPACT data file after optimization, an analysis run, and a schematic of the optimized push-pull output network. Note that C1 is a single 43 pF capacitor instead of two 87.5 pF capacitors in series. Closest standard value capacitors are used.

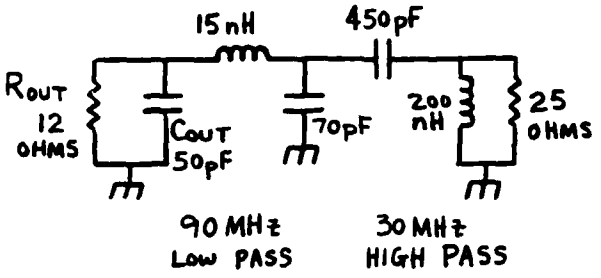


Figure 2.12-4 L-C Output Network Before Optimization

```
* DISCRETE DV2880V 40W 28V MATCHING NETWORK
BLK
 TRF 1 2 N=1.414
 IND 2 0 L=?139.08NH?
 CAP 2 3 C=?307.79PF?
 CAP 3 0 C=?87.466PF?
 IND 3 4 L=?31.028NH?
 CAP 4 0 C=50PF
 RES 4 0 R=12
NET:1POR 1
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI NET S
END
OPT
 NET MS11=-20DB
END
```

```
CIRCUIT:  NET
ONE-PORT, ZS =    50. +J     0.
   FREQ              RHO                SWR       RET L/G
    MHZ        MAG        ANG                       dB
  30.00000    0.101      6.2       1.22:1      -19.91
  40.00000    0.088   -147.6       1.19:1      -21.07
  50.00000    0.133   -177.1       1.31:1      -17.52
  60.00000    0.128    161.9       1.29:1      -17.87
  70.00000    0.096    134.3       1.21:1      -20.32
  80.00000    0.071     78.0       1.15:1      -22.93
  90.00000    0.116     16.4       1.26:1      -18.69
```

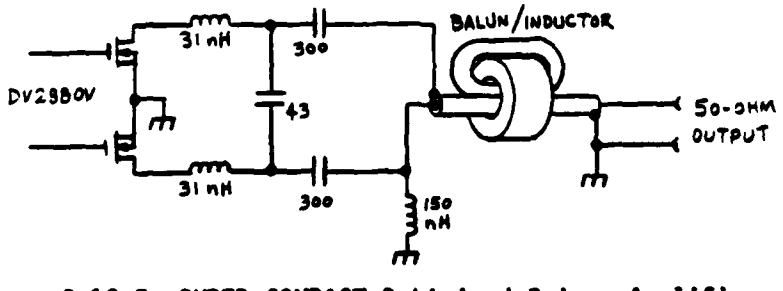
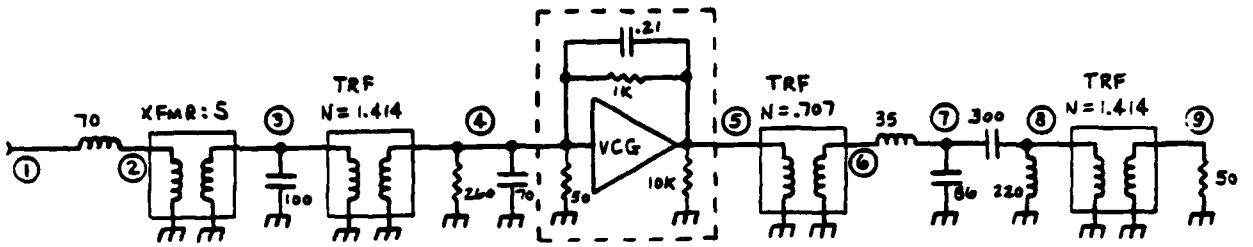


Figure 2.12-5 SUPER-COMPACT Optimized Driver Amplifier
Output Matching Network Data File And Schematic

The next step was to model the input network of the test amplifier in an attempt to improve the input match for higher gain. S-parameters were measured on a variety of impedance matching transformers before amplifier testing began, so data was available for the model. Figure 2.12-6 is the model resulting from the SUPER-COMPACT session, including the schematic, a data file listing, and an analysis run. With a reasonable model of the input impedance of the DV2880V, a new input network was designed and optimized. As shown in Figure 2.12-7, the input VSWR of the L-C circuit model is much lower than that of the transformer-based breadboard circuit.

Testing of a breadboard version of the computer-optimized amplifier revealed a surprising characteristic of push-pull circuits. Although the matching networks present a low-VSWR differential-mode load impedance to the DV2880V, the bifilar-wound gate and drain bias inductors appear as short circuits in the common-mode circuit, causing a 50 MHz common-mode oscillation. Stable common-mode loads were empirically determined by installing series resistors in the center-tap leads of the bias inductors, with a DC feed choke across the drain resistor to handle the current. Eliminating the common-mode oscillation problem in this manner allows much higher value gate-to-ground resistors than the typical 5-to-10 ohm range seen in application circuits. The result is more stable operation, higher power gain, and simplified input matching networks. A slight amount of drain-to-gate feedback was retained to ensure stability into the relatively high VSWR of the six-way RF power splitter driving the six output RF amplifiers. From small-signal S-parameter data, the amplifier was found to be potentially unstable at 110 MHz when driving a load with a reflection coefficient of 0.83 or higher, but the splitter reflection coefficient at 110 MHz is 0.56. Shown schematically in Figure 2.12-8, the complete driver dual has component values very close to the computer optimized circuit, even after tuning to compensate for component and layout effects.

Tables 2.12-2 thru 2.12-4 list 50-ohm performance data for the breadboard driver amplifier halves, and for the quad-combined dual. In all cases, the gate-to-source control voltage is +5.0 VDC, and the drain power supply voltage is +28 VDC. Table 2.12-5 is a driver dual VSWR-performance summary. All data was taken at 2.5 watts drive, so the amplifier was operating at maximum gain, and no spurious outputs were present. The photographs in Figures 2.12-9 and 2.12-10 show the spectral output of the breadboard driver dual powered by the breadboard switching power supply. The performance, already very close to that specified will improve in the final layout with improved shielding and a concentrated effort to improve broadband bypassing and decoupling.

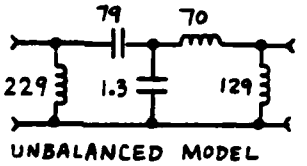



```
* MODEL OF BREADBOARD DV2880V DRIVER WITH 3T XFORMER
BLK
 IND 1 2 L=70NH
 TWO 2 3 XFMR
 CAP 3 0 C=100PF
 TRF 3 4 N=1.414
RES 4 0 R=?259.99?
 CAP 4 0 C=?94.441PF?
 VCG 4 5 G=?9.1768E-3? R1=50 R2=10000
 RES 4 5 R=1000
 CAP 4 5 C=?.21114PF?
 TRF 5 6 N=.707
 IND 6 7 L=35NH
 CAP 7 0 C=86PF
 CAP 7 8 C=300PF
 IND 8 0 L=220NH
 TRF 8 9 N=1.414
INPUT:1POR 1
END
DATA
XFMR:S
 .82 11 .57 0 .57 0 .82 172
 .82 6 .57 -4 .57 -4 .81 168
 .81 3 .57 -6 .57 -6 .82 166
 .81 0 .56 -9 .56 -9 .81 164
 .81 -2 .56 -12 .56 -12 .82 161
 .81 -5 .55 -14 .55 -14 .82 158
 .80 -7 .55 -17 .55 -17 .82 155
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI INPUT S
END
OPT
 INPUT F=30MHZ MS11=-1.5DB
 INPUT F=40MHZ MS11=-2.3DB
 INPUT F=50MHZ MS11=-3.0DB
 INPUT F=60MHZ MS11=-4.1DB
 INPUT F=70MHZ MS11=-5.7DB
 INPUT F=80MHZ MS11=-6.0DB
 INPUT F=90MHZ MS11=-10.0DB
END
```

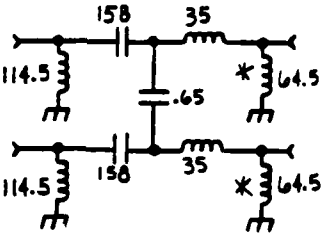
```
CIRCUIT:  INPUT
ONE-PORT, ZS =   50. +J    0.
   FREQ          RHO                SWR      RET L/G
    MHZ       MAG       ANG                    dB
  30.00000   0.844    -6.9      11.83:1      -1.47
  40.00000   0.789   -22.1       8.48:1      -2.06
  50.00000   0.733   -37.3       6.48:1      -2.70
  60.00000   0.589   -58.5       3.87:1      -4.59
  70.00000   0.392  -105.9       2.29:1      -8.14
  80.00000   0.342   166.9       2.04:1      -9.31
  90.00000   0.597   100.0       3.96:1      -4.48
```

Figure 2.12-6 Breadboard Driver Amplifier Model Schematic And Data File

```
BLK
 IND 1 0 L=?228.97NH?
 CAP 1 2 C=?79.172PF?
 CAP 2 0 C=?1.3193PF?
 IND 2 3 L=?70.179NH?
 IND 3 0 L=?129.41NH?
 TRF 3 4 N=1.414
 RES 4 0 R=50
 CAP 4 0 C=94.441PF
 VCG 4 5 G=9.1768E-3 R1=260 R2=10000
 RES 4 5 R=1000
 CAP 4 5 C=.21114PF
 TRF 5 6 N=.707
 IND 6 7 L=35NH
 CAP 7 0 C=86PF
 CAP 7 8 C=300PF
 IND 8 0 L=220NH
 TRF 8 9 N=1.414
INPUT:1POR 1
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI INPUT S
END
OPT
 INPUT F=30MHZ MS11=-10DB
 INPUT F=40MHZ MS11=-10DB
 INPUT F=50MHZ MS11=-10DB
 INPUT F=60MHZ MS11=-10DB
 INPUT F=70MHZ MS11=-10DB
 INPUT F=80MHZ MS11=-15DB
 INPUT F=90MHZ MS11=-20.0DB
END
CMD > ANA
```

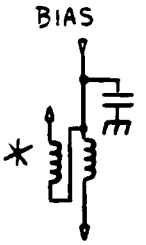


UNBALANCED MODEL



BALANCED EQUIVALENT CIRCUIT

OR




```
CIRCUIT:  INPUT
ONE-PORT, ZS =   50. +J    0.
```

FREQ	RHO		SWR	RET L/G	Ohms	
MHZ	MAG	ANG		dB	R	X
30.00000	0.332	-70.9	1.99:1	-9.57	49.8	-35.2
40.00000	0.477	145.9	2.82:1	-6.43	19.1	13.3
50.00000	0.501	110.0	3.01:1	-6.00	23.5	29.6
60.00000	0.427	80.7	2.49:1	-7.39	39.1	40.4
70.00000	0.311	52.1	1.90:1	-10.15	63.2	34.3
80.00000	0.173	13.3	1.42:1	-15.22	70.0	5.7
90.00000	0.109	-80.2	1.25:1	-19.23	50.7	-11.0

Figure 2.12-7 Optimized Driver Amplifier L-C Input Network Data File

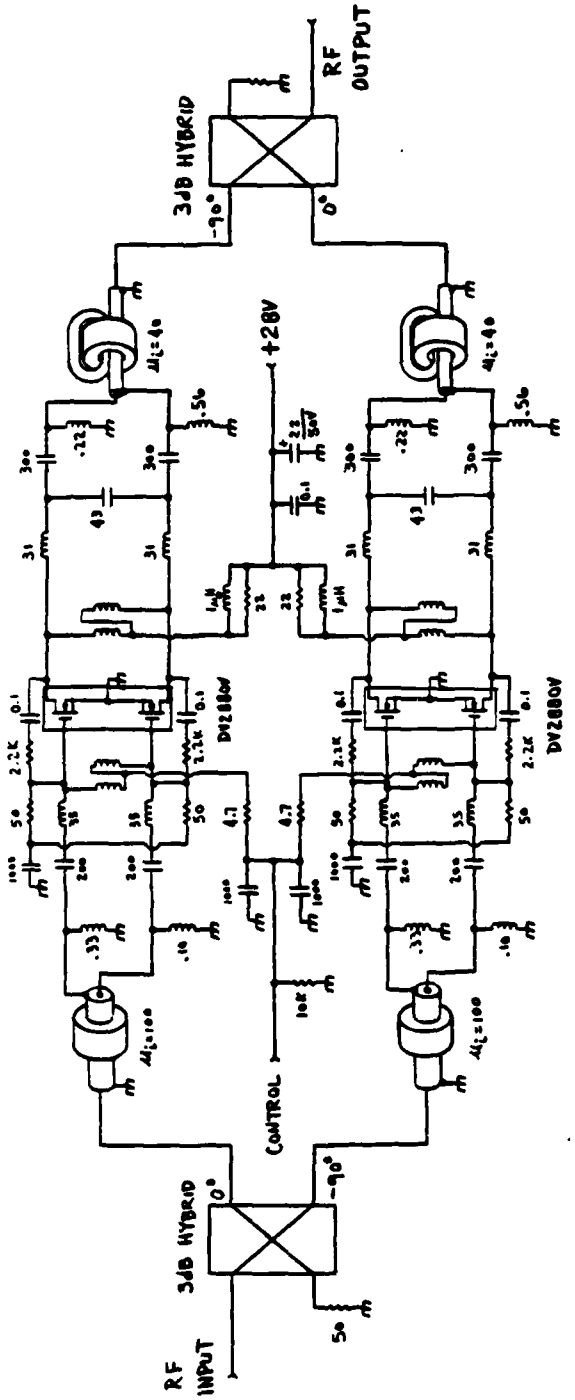


Figure 2.12-8 RF Driver Amplifier Schematic

Table 2.12-2 Driver Amplifier 50-Ohm Test Data - Side 1

DV2880V MOSFET DRIVER AMP (Vgs=5.0v)

FREQ. (MHz)	P (OUT) (WATTS)	P (FWD) (WATTS)	P (REF) (WATTS)	GAIN (dB)	I (AMPS)	EFFICIENCY (%)
90	35.000	0.960	0.486	15.62	2.865	43.64
89	35.000	0.951	0.449	15.66	2.869	43.57
88	35.000	0.944	0.424	15.69	2.686	43.32
87	35.000	0.936	0.399	15.73	2.912	42.92
86	35.000	0.929	0.373	15.76	2.932	42.63
85	35.000	1.037	0.342	15.28	2.934	42.60
84	35.000	1.029	0.318	15.32	2.955	42.30
83	35.000	1.021	0.288	15.35	2.953	42.33
82	35.000	1.015	0.264	15.38	2.969	42.10
81	35.000	1.007	0.242	15.41	2.987	41.85
80	35.000	1.000	0.219	15.44	2.992	41.78
79	35.000	0.994	0.196	15.47	2.998	41.69
78	35.000	0.988	0.178	15.49	3.026	41.31
77	35.000	0.981	0.154	15.53	3.013	41.49
76	35.000	1.084	0.138	15.09	3.034	41.20
75	35.000	1.077	0.121	15.12	3.046	41.04
74	35.000	1.071	0.030	15.14	3.042	41.10
73	35.000	1.066	0.099	15.16	3.041	41.10
72	35.000	1.060	0.089	15.19	3.061	40.84
71	35.000	1.055	0.070	15.21	3.052	40.96
70	35.000	1.051	0.062	15.22	3.073	40.68
69	35.000	1.045	0.046	15.25	3.063	40.80
68	35.000	1.042	0.036	15.26	3.066	40.77
67	35.000	1.141	0.028	14.87	3.080	40.58
66	35.000	1.137	0.024	14.88	3.071	40.70
65	35.000	1.134	0.019	14.89	3.076	40.64
64	35.000	1.129	0.016	14.91	3.089	40.47
63	35.000	1.126	0.014	14.92	3.092	40.43
62	35.000	1.124	0.015	14.93	3.104	40.27
61	35.000	1.123	0.014	14.94	3.088	40.48
60	35.000	1.219	0.022	14.58	3.087	40.50
59	35.000	1.219	0.030	14.58	3.103	40.28
58	35.000	1.216	0.041	14.59	3.090	40.46
57	35.000	1.215	0.053	14.60	3.090	40.45
56	35.000	1.215	0.067	14.60	3.080	40.58
55	35.000	1.318	0.083	14.24	3.086	40.51
54	35.000	1.319	0.105	14.24	3.075	40.65
53	35.000	1.321	0.112	14.23	3.062	40.82
52	35.000	1.324	0.129	14.22	3.049	41.00
51	35.000	1.325	0.147	14.22	3.022	41.37
50	35.000	1.330	0.171	14.20	3.016	41.45
49	35.000	1.333	0.193	14.19	2.998	41.70
48	35.000	1.337	0.213	14.18	2.964	42.16
47	35.000	1.343	0.239	14.16	2.949	42.39
46	35.000	1.350	0.265	14.14	2.937	42.57
45	35.000	1.357	0.291	14.11	2.925	42.73
44	35.000	1.365	0.312	14.09	2.902	43.07
43	35.000	1.373	0.338	14.06	2.899	43.13
42	35.000	1.385	0.355	14.03	2.878	43.44
41	35.000	1.396	0.372	13.99	2.860	43.71
40	35.000	1.410	0.392	13.95	2.850	43.86
39	35.000	1.314	0.397	14.25	2.817	44.38
38	36.000	1.330	0.404	14.32	2.824	45.53
37	35.000	1.348	0.393	14.14	2.807	44.54
36	35.000	1.253	0.372	14.46	2.757	45.33
35	35.000	1.271	0.353	14.40	2.740	45.62
34	35.000	1.293	0.335	14.32	2.743	45.58
33	35.000	1.296	0.310	14.66	2.741	45.60
32	35.000	1.221	0.285	14.57	2.742	45.60
31	35.000	1.247	0.269	14.44	2.776	45.04
30	35.000	1.277	0.270	14.38	2.802	44.62

Table 2.12-3 Driver Amplifier 50-Ohm Test Data - Side 2

VHF AMPLIFIER TEST DATA

DV2880V MOSFET DRIVER AMP (Vgs=5.0V)

FREQ. (MHz)	P (OUT) (mWATTS)	P (FWD) (mWATTS)	P (REF) (mWATTS)	GAIN (dB)	I (AMPS)	EFFICIENCY (%)
90	35.000	0.720	0.333	16.87	3.129	39.95
89	35.000	0.713	0.285	16.78	3.072	39.53
88	35.000	0.706	0.289	16.94	3.128	39.96
87	35.000	0.702	0.270	16.98	3.129	39.95
86	35.000	0.697	0.255	17.01	3.141	39.80
85	35.000	0.691	0.237	17.04	3.139	39.82
84	35.000	0.686	0.222	17.08	3.149	39.70
83	35.000	0.681	0.201	17.11	3.142	39.79
82	35.000	0.769	0.191	16.47	3.161	39.55
81	35.000	0.784	0.176	16.50	3.169	39.45
80	35.000	0.778	0.161	16.53	3.170	39.44
79	35.000	0.773	0.140	16.56	3.170	39.44
78	35.000	0.768	0.131	16.59	3.182	39.28
77	35.000	0.763	0.122	16.62	3.190	39.18
76	35.000	0.759	0.102	16.64	3.193	39.15
75	35.000	0.754	0.097	16.67	3.192	39.16
74	35.000	0.750	0.090	16.69	3.199	39.08
73	35.000	0.746	0.080	16.71	3.191	39.17
72	35.000	0.742	0.075	16.74	3.204	39.02
71	35.000	0.739	0.064	16.76	3.211	38.93
70	35.000	0.841	0.057	16.19	3.211	38.93
69	35.000	0.836	0.049	16.22	3.217	38.74
68	35.000	0.833	0.042	16.23	3.229	38.71
67	35.000	0.829	0.037	16.25	3.228	38.72
66	35.000	0.827	0.033	16.27	3.234	38.66
65	35.000	0.825	0.029	16.28	3.227	38.73
64	35.000	0.821	0.027	16.30	3.237	38.62
63	35.000	0.819	0.022	16.31	3.227	38.74
62	35.000	0.817	0.023	16.32	3.233	38.66
61	35.000	0.917	0.025	15.82	3.245	38.52
60	35.000	0.914	0.030	15.83	3.239	38.59
59	35.000	0.914	0.034	15.83	3.231	38.69
58	35.000	0.912	0.039	15.84	3.249	38.48
57	35.000	0.911	0.049	15.84	3.258	38.37
56	35.000	0.911	0.055	15.84	3.256	38.40
55	35.000	1.014	[illegible]	15.36	3.255	38.40
54	35.000	1.015	0.076	15.36	3.266	38.28
53	35.000	1.016	0.090	15.37	3.254	38.42
52	35.000	1.016	0.101	15.36	3.250	38.46
51	35.000	1.019	0.118	15.36	3.258	38.37
50	35.000	1.023	0.127	15.34	3.248	38.48
49	35.000	1.025	0.144	15.33	3.245	38.52
48	35.000	1.029	0.159	15.32	3.225	38.77
47	35.000	1.033	0.182	15.30	3.233	38.66
46	35.000	1.038	0.200	15.28	3.237	38.61
45	35.000	1.044	0.207	15.25	3.219	38.84
44	35.000	1.050	0.216	15.23	3.196	39.11
43	35.000	0.951	0.217	15.66	3.160	39.55
42	35.000	0.959	0.233	15.62	3.147	39.72
41	35.000	0.967	0.240	15.59	3.117	40.11
40	35.000	0.976	0.248	15.55	3.096	40.37
39	35.000	0.986	0.250	15.50	3.077	40.63
38	35.000	0.998	0.249	15.45	3.050	40.99
37	35.000	0.899	0.240	15.90	3.000	41.67
36	35.000	0.911	0.234	15.84	2.965	42.16
35	35.000	0.924	0.236	15.78	2.962	42.21
34	35.000	0.940	0.232	15.83	2.944	43.68
33	35.000	0.957	0.221	15.63	2.921	42.80
32	35.000	0.977	0.217	15.54	2.909	42.98
31	35.000	1.123	0.234	14.94	2.898	43.14
30	35.000	1.405	0.253	13.96	2.883	43.36

Table 2.12-4 Driver Amplifier 50-Ohm Test Data

VHF AMPLIFIER TEST DATA

CV2880V MOSFET DRIVER AMP (VGS=5.0V)

FREQ. (MHz)	P (OUT) (WATTS)	P (FWD) (WATTS)	P (REF) (WATTS)	GAIN (dB)	I (AMPS)	EFFICIENCY (%)
90	60.000	2.040	0.002	14.69	5.945	36.05
89	60.000	2.021	0.001	14.73	5.967	35.91
88	60.000	2.005	0.001	14.76	5.966	35.92
87	60.000	1.990	0.000	14.79	5.969	35.90
86	60.000	1.974	0.000	14.83	6.002	35.70
85	60.000	1.959	0.000	14.86	5.959	35.96
84	60.000	1.944	0.000	14.89	5.979	35.84
83	60.000	1.929	0.000	14.93	5.975	35.86
82	60.000	2.030	0.001	14.71	6.018	35.61
81	60.000	2.015	0.001	14.74	6.033	35.52
80	60.000	2.000	0.001	14.77	6.035	35.51
79	60.000	1.986	0.001	14.80	6.018	35.61
78	60.000	1.976	0.001	14.82	6.016	35.62
77	60.000	1.961	0.001	14.86	6.038	35.49
76	60.000	1.952	0.001	14.88	6.024	35.57
75	60.000	1.938	0.000	14.91	6.026	35.56
74	60.000	2.036	0.000	14.69	6.042	35.47
73	60.000	1.919	0.000	14.95	6.003	35.69
72	60.000	2.014	0.000	14.74	6.046	35.44
71	60.000	2.005	0.001	14.76	6.002	35.70
70	60.000	1.996	0.001	14.78	6.000	35.72
69	60.000	1.986	0.002	14.80	6.035	35.51
68	60.000	1.979	0.003	14.82	6.024	35.57
67	60.000	1.970	0.004	14.84	6.016	35.62
66	60.000	1.963	0.005	14.85	5.990	35.77
65	60.000	1.959	0.006	14.86	6.005	35.69
64	60.000	2.053	0.009	14.66	6.015	35.63
63	60.000	2.048	0.011	14.67	5.961	35.83
62	60.000	2.043	0.013	14.68	6.000	35.71
61	60.000	2.039	0.014	14.69	5.999	35.72
60	60.000	2.133	0.015	14.49	6.014	35.63
59	60.000	2.032	0.014	14.70	5.986	35.80
58	60.000	2.128	0.020	14.50	6.011	35.65
57	60.000	2.126	0.021	14.51	6.011	35.65
56	60.000	2.126	0.022	14.51	5.999	35.72
55	60.000	2.027	0.021	14.71	5.943	36.06
54	60.000	2.131	0.022	14.50	5.980	35.83
53	60.000	2.133	0.021	14.49	5.980	35.83
52	60.000	2.138	0.017	14.48	5.960	35.95
51	60.000	2.140	0.017	14.48	5.956	35.98
50	60.000	2.250	0.016	14.26	5.947	36.03
49	60.000	2.255	0.018	14.25	5.962	35.94
48	60.000	2.160	0.014	14.44	5.907	36.27
47	60.000	2.273	0.021	14.21	5.945	36.04
46	60.000	2.284	0.018	14.19	5.920	36.20
45	60.000	2.193	0.019	14.37	5.872	36.49
44	60.000	2.205	0.019	14.35	5.874	36.48
43	60.000	2.218	0.023	14.32	5.836	36.72
42	60.000	2.237	0.029	14.29	5.832	36.75
41	60.000	2.363	0.036	14.05	5.812	36.87
40	61.000	2.386	0.053	14.06	5.635	37.34
39	60.000	2.409	0.053	13.96	5.814	36.86
38	60.000	2.439	0.051	13.91	5.816	36.85
37	60.000	2.584	0.092	13.66	5.846	36.64
36	60.000	2.620	0.099	13.60	5.826	36.78
35	60.000	2.542	0.095	13.73	5.791	37.00
34	60.000	2.703	0.117	13.46	5.807	36.90
33	60.000	2.750	0.126	13.39	5.783	37.06
32	60.000	2.932	0.135	13.13	5.757	37.22
31	60.000	3.367	0.146	12.51	5.758	37.21
30	60.000	* 4.088	0.215	11.67	5.743	37.31

Table 2.12-5 Driver Dual VSWR Performance Summary (P_{IN} = 2.5 W)

	FREQUENCY (MHz)						
	30	40	50	60	70	80	88
VSWR	6:1	5:1	4:1	3:1	2:1	2:1	1:1
P_{OUT} (W)	15	25	40	45	60	60	75
MAXIMUM							
I_{TOTAL} (A)	3.2	3.5	4.8	5.3	6.2	6.3	6.7
V_{gs} (V)	2.8	3.0	4.0	4.1	4.7	4.7	5.0
MINIMUM							
I_{TOTAL} (A)	2.0	2.8	4.1	4.6	5.5	5.3	N/A
V_{gs} (V)	1.6	2.5	3.1	3.2	3.8	3.5	N/A

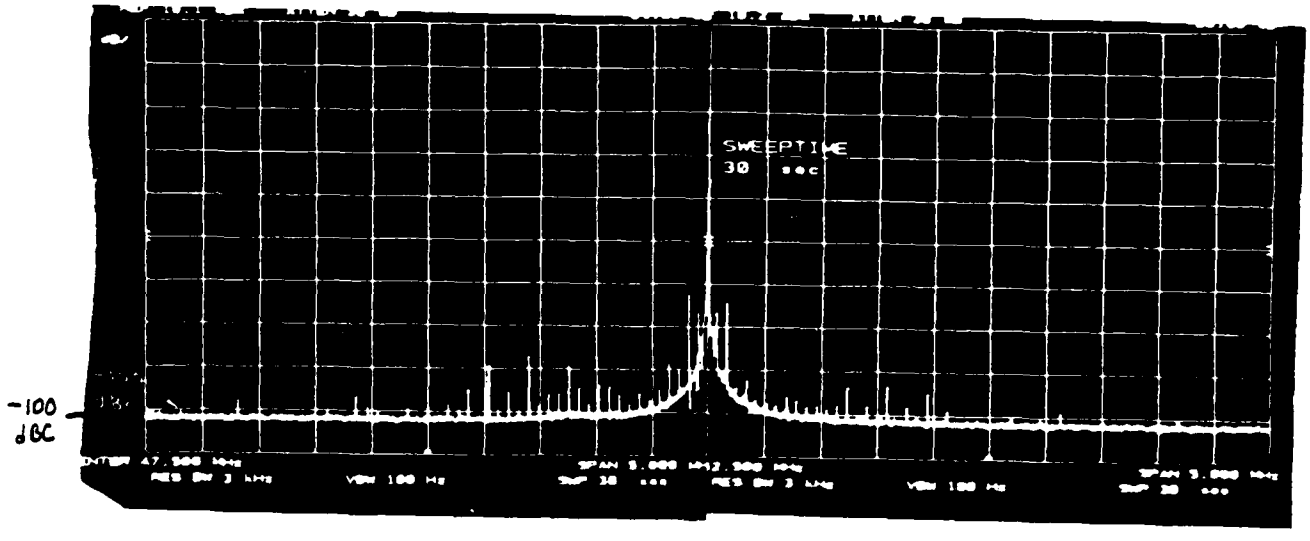


Figure 2.12-9 Spurious Outputs About A 50 MHz Carrier (± 5 MHz)

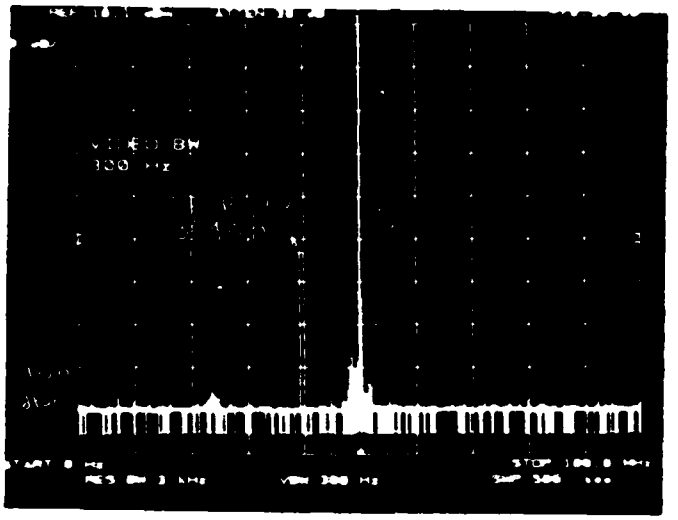


Figure 2.12-10 Spurious Outputs From DC To 100 MHz

In testing of the breadboard 500-watt power amplifier, the RF driver amplifier has proven itself to be a stable, dependable RF power source featuring low input VSWR and high-speed AGC capability.

2.13 RF OUTPUT AMPLIFIER (A12-A17)

The RF output amplifier assembly provides the gain and output power capability to overcome losses in the output circuits and achieve the 500-watt output level required. This assembly must be capable of operating into the load VSWR of the antenna system, which at VHF is relatively uncontrolled and typically ranges up to 5:1. Since the amplifier is to be used in a moving vehicle, the load will vary with time and position of the vehicle. Further, the amplifier module includes an integral power supply regulator to isolate the RF amplifier from the widely-varying vehicular supply and to provide the required voltages for the amplifier and its bias source.

Six output amplifiers are paralleled to achieve the required output. A combiner and splitter provide the necessary isolation between amplifiers and also phase-stagger the load impedance seen by each amplifier. Therefore, when operating into high load VSWR's, amplifiers saturated because of the load presented are compensated by other amplifiers of the set, and the full required output is obtained. The switching transients at the power amplifier are also phase-staggered to reduce switching transients at the power amplifier input and reduce conducted emissions.

2.13.1 RF Amplifier Design

Based on the Motorola MRF317, the amplifier input and output matching networks were designed using impedance data interpolated from published source and load impedances. Because of the very low impedances of the transistors, transformer matching networks are required for the desired broadband performance. Before initiating the amplifier design, a variety of ferrite-loaded matching transformers were constructed, and accuracy-improved S-parameter data was taken. These transformers were the building blocks of the computer-optimized matching networks investigated. Ferrite cores with initial permeabilities of 40, 100 and 240 were evaluated in transformers, and only the permeability of 40 cores were acceptable for use in the RF output amplifier because of the high insertion losses of the higher permeability cores.

After computer analysis of a number of input and output matching networks, an amplifier design employing 3-turn input and output transformers was chosen for construction and testing. The SUPER-COMPACT input and output data files and analysis runs appear in Tables 2.13.1-1 and 2.13.1-2, respectively. The output transformer is constructed from larger ferrite cores than the input transformer to handle the higher power levels present. A breadbard amplifier was constructed and tested. Performance was inadequate because, due to the physical size of the transistors and the output transformer, the series output inductance could not be reduced enough to achieve the predicted performance. A schematic of the amplifier appears in Figure 2.13.1-1.

Table 2.13.1-1 Input Network With 3-Turn Transformer-
Data File Listing And Analysis

```
LAD
 CAP 1 0 C=4.7PF
IND 1 2 L=115NH
 CAP 2 0 C=43PF
 TWO 2 3 XFMR
 SLC 3 0 L=.6NH C=253PF
 IND 3 4 L=5.7NH
 SLC 4 0 L=.6NH C=395PF
 IND 4 5 L=7.5NH
 TRF 5 6 N=1.414
 ONE 6 0 MRF317
 INPUT:1POR 1
END
DATA
 MRF317:S
.953 -175
.957 -176
.961 -176
.969 -177
.976 -178
.982 -179
.988 180
END
DATA
 XFMR:S
.82 11 .57 0 .57 0 .82 172
.82 6 .57 -4 .57 -4 .81 168
.81 3 .57 -6 .57 -6 .82 166
.81 0 .56 -9 .56 -9 .81 164
.81 -2 .56 -12 .56 -12 .82 161
.81 -5 .55 -14 .55 -14 .82 158
.80 -7 .55 -17 .55 -17 .82 155
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI INPUT S
END
OPT
 INPUT F=30MHZ MS11=-3DB
 INPUT F=40MHZ MS11=-3DB
 INPUT F=50MHZ MS11=-4DB
 INPUT F=60MHZ MS11=-5DB
 INPUT F=70MHZ MS11=-6DB
 INPUT F=80MHZ MS11=-7DB
 INPUT F=90MHZ MS11=-20DB
END
```

FREQ	RHO		SWR	RET L/G
MHZ	MAG	ANG		DB
30.00000	0.659	96.8	4.86:1	-3.62
40.00000	0.692	36.5	5.49:1	-3.20
50.00000	0.732	2.7	6.46:1	-2.71
60.00000	0.647	-55.7	4.66:1	-3.78
70.00000	0.623	-133.3	4.31:1	-4.11
80.00000	0.551	137.4	3.45:1	-5.18
90.00000	0.276	-98.4	1.76:1	-11.20

Table 2.13.1-2 Output Network With 3-Turn Transformer-
Data File Listing And Analysis

```
LAB
 CAP 1 0 C=?3.0135PF?
 IND 1 2 L=?134.57NH?
 CAP 2 0 C=?30.279PF?
 TWO 2 3 XFMR
 SLC 3 0 L=.6NH C=?6.2381PF?
 IND 3 4 L=2NH
 CAP 4 0 C=?2.8132PF?
 IND 4 5 L=.1NH
 TRF 5 6 N=1.414
 ONE 6 0 MRF317
 INPUT:1POR 1
END
DATA
 MRF317:S
.843 -168
.846 -169
.853 -169
.867 -169
.888 -170
.902 -172
.916 -173
END
DATA
 XFMR:S
.827 11 .56 0 .56 0 .828 171
.828 6 .56 -4 .56 -4 .828 168
.828 2 .56 -8 .56 -8 .828 165
.828 -2 .56 -11 .56 -11 .829 161
.829 -4 .56 -14 .56 -14 .830 156
.828 -7 .55 -17 .55 -17 .833 155
.825 -11 .54 -21 .54 -21 .835 151
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI INPUT S
END
OPT
 INPUT  MS11=-20DB
END
```

FREQ	RHO		SWR	RET L/G	Ohms	
MHZ	MAG	ANG		dB	R	X
30.00000	0.379	-67.8	2.22:1	-8.44	50.0	-40.9
40.00000	0.204	-98.6	1.51:1	-13.82	43.5	-18.3
50.00000	0.103	-168.9	1.23:1	-19.74	40.8	-1.6
60.00000	0.180	110.1	1.44:1	-14.92	41.9	14.6
70.00000	0.243	49.3	1.64:1	-12.30	63.4	24.8
80.00000	0.173	-1.1	1.42:1	-15.26	70.9	-0.5
90.00000	0.232	-155.2	1.60:1	-12.69	32.1	-6.6

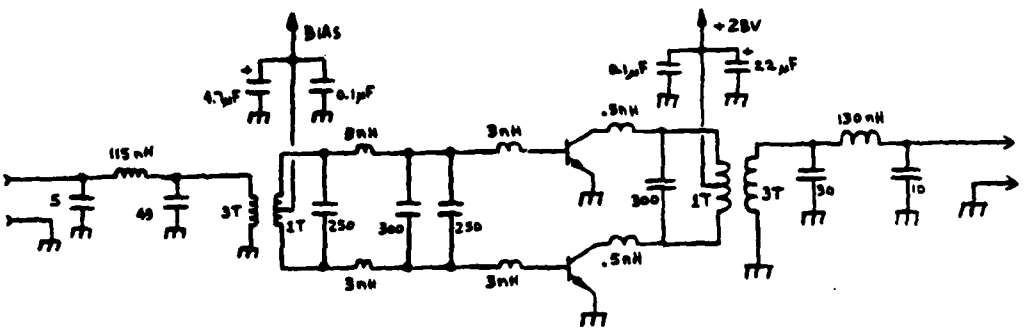


Figure 2.13.1-1 Schematic Of Output Dual With 3-Turn Output Transformer

Another transformer, a 4:1 coaxial configuration, was tested in the computer model, and the optimized data file and an analysis run appear in Table 2.13.1-3. The optimized circuit model employs 12 nH of inductance between the collectors and the transformer, compared to 2 nH in the 3-turn transformer circuit, making the new circuit realizable. Replacing the output network of the breadboard amplifier with the revised circuit made a drastic improvement in the performance. Tuning component values to allow for layout effects on the low impedance amplifier circuitry yielded an excellent 125-watt broadband amplifier meeting the requirements for use in the 500-watt VHF PA. The addition of feedback improved the input match and the stability of the amplifier as indicated by analysis of small-signal S-parameter data. Figure 2.13.1-2 is a schematic of the final circuit configuration of the RF output amplifier. Table 2.13.1-4 is a computer printout of automatic test data taken every 1 MHz on amplifier #001 before installation on the breadboard 500-watt amplifier heatsink. The base-bias voltage was adjusted to 0.55 VDC.

Table 2.13.1-3 Output Network With 4:1 Coaxial Transformer-
Data File And Analysis

```
LAD
 CAP 1 0 C=?36.09BPF?
 IND 1 2 L=.1NH
 CAP 2 0 C=.1PF
 TWO 2 3 XFMR
 SLC 3 0 L=.6NH C=?15PF?
 IND 3 4 L=.1NH
 CAP 4 0 C=.1PF
 IND 4 5 L=?12NH?
 TRF 5 6 N=1.414
 ONE 6 0 MRF317
 INPUT:1POR 1
END
DATA
 MRF317:S
.843 -168
.846 -169
.853 -169
.867 -169
.888 -170
.902 -172
.916 -173
END
DATA
 XFMR:S
.643 34 .76 10 .76 10 .646 168
.630 25 .77 6 .77 6 .633 168
.624 18 .78 2 .78 2 .625 168
.619 13 .78 -1 .78 -1 .621 166
.615 10 .79 -3 .79 -3 .619 165
.608 6 .79 -5 .79 -5 .617 164
.601 4 .79 -7 .79 -7 .616 163
END
FREQ
 STEP 30MHZ 90MHZ 10MHZ
END
OUT
 PRI INPUT S
END
OPT
 INPUT MS11=-20DB
END
```

FREQ	RHO		SWR	RET L/G	Ohms	
MHZ	MAG	ANG		dB	R	X
30.00000	0.346	-106.7	2.06:1	-9.23	33.4	-25.1
40.00000	0.352	-124.8	2.08:1	-9.08	28.7	-18.9
50.00000	0.364	-137.9	2.14:1	-8.79	26.0	-14.6
60.00000	0.345	-152.6	2.05:1	-9.25	25.5	-9.2
70.00000	0.307	179.4	1.89:1	-10.24	26.5	0.2
80.00000	0.169	123.3	1.41:1	-15.43	40.0	11.7
90.00000	0.231	36.8	1.60:1	-12.73	69.3	20.2

Table 2.13.1-4 Output Dual 125-Watt Performance Data

FREQ. (MHz)	P (OUT) (WATTS)	P (FWD) (WATTS)	P (REF) (WATTS)	GAIN (DB)	I (AMPS)	EFFICIENCY (%)
90	126.000	8.376	0.702	11.47	7.145	62.98
89	125.000	8.182	0.310	11.84	7.137	62.55
88	125.000	7.643	0.131	12.14	7.164	62.31
87	125.000	7.461	0.124	12.24	7.174	62.23
86	125.000	7.297	0.242	12.34	7.159	62.36
85	125.000	7.347	0.449	12.31	7.194	62.06
84	125.000	7.529	0.714	12.20	7.206	61.96
83	125.000	7.638	1.017	12.11	7.217	61.86
82	125.000	7.665	1.353	12.01	7.226	61.78
81	125.000	8.141	1.706	11.85	7.245	61.62
80	125.000	8.304	2.044	11.73	7.267	61.43
79	126.000	8.472	2.383	11.72	7.306	61.60
78	125.000	8.639	2.672	11.60	7.297	61.18
77	126.000	8.903	3.012	11.51	7.335	61.35
76	126.000	9.076	3.299	11.42	7.365	61.10
75	125.000	9.226	3.521	11.32	7.362	60.64
74	125.000	9.299	3.764	11.28	7.394	60.37
73	126.000	9.457	3.962	11.25	7.409	60.74
72	125.000	9.507	4.118	11.19	7.413	60.22
71	125.000	9.568	4.309	11.16	7.434	60.05
70	126.000	9.628	4.444	11.17	7.458	60.34
69	125.000	9.583	4.539	11.15	7.475	59.73
68	125.000	9.539	4.622	11.17	7.479	59.69
67	126.000	9.610	4.732	11.18	7.538	59.70
66	125.000	9.474	4.753	11.20	7.571	58.97
65	125.000	9.339	4.737	11.27	7.586	58.85
64	125.000	9.102	4.683	11.38	7.571	58.97
63	125.000	8.868	4.614	11.49	7.555	59.09
62	126.000	8.644	4.523	11.64	7.548	59.62
61	126.000	8.431	4.443	11.74	7.500	60.00
60	126.000	8.108	4.327	11.91	7.483	60.14
59	125.000	7.888	4.206	12.00	7.461	59.83
58	125.000	7.576	4.116	12.17	7.436	60.04
57	126.000	7.355	4.026	12.33	7.408	60.74
56	125.000	7.164	3.937	12.42	7.381	60.48
55	125.000	6.970	3.834	12.54	7.329	60.91
54	125.000	6.768	3.731	12.66	7.308	61.09
53	126.000	6.573	3.706	12.83	7.263	61.96
52	125.000	6.378	3.615	12.92	7.200	62.01
51	125.000	6.183	3.555	13.05	7.123	62.68
50	125.000	6.102	3.498	13.11	7.075	63.10
49	125.000	5.919	3.457	13.25	7.049	63.33
48	125.000	5.735	3.363	13.38	6.966	64.09
47	125.000	5.658	3.342	13.44	6.955	64.19
46	125.000	5.477	3.288	13.58	6.933	64.40
45	125.000	5.301	3.217	13.73	6.919	64.53
44	125.000	5.221	3.169	13.79	6.937	64.36
43	125.000	5.053	3.125	13.93	6.962	64.13
42	125.000	4.933	3.070	13.99	6.995	63.82
41	125.000	4.810	3.013	14.15	6.974	64.02
40	125.000	4.640	2.948	14.30	6.949	64.24
39	125.000	4.473	2.844	14.46	6.921	64.50
38	125.000	4.391	2.749	14.75	6.890	64.80
37	125.000	4.021	2.567	14.93	6.858	65.10
36	125.000	3.850	2.560	15.11	6.814	65.51
35	125.000	3.673	2.466	15.31	6.792	65.73
34	125.000	3.507	2.362	15.52	6.759	66.05
33	125.000	3.215	2.243	15.90	6.729	66.34
32	125.000	3.036	2.161	16.15	6.735	66.28
31	125.000	2.854	2.040	16.41	6.724	66.39
30	125.000	2.794	1.930	16.51	6.812	65.54

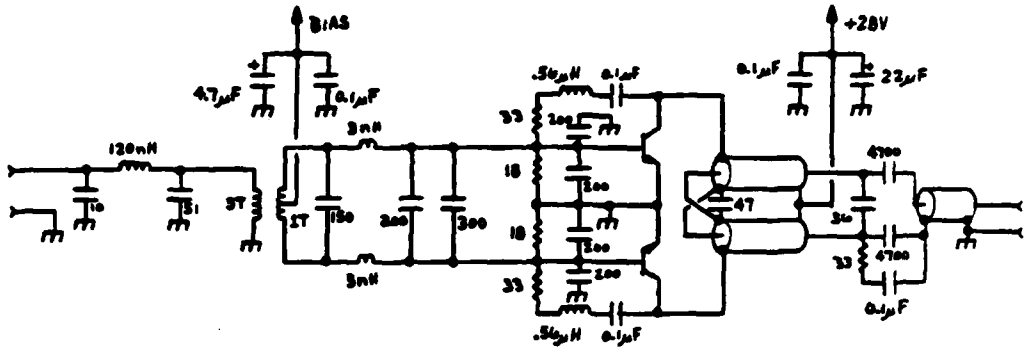


Figure 2.13.1-2 Schematic Of Output Dual With 4:1 Coaxial Output Transformer

Stability predictions for the RF output amplifiers are based on small-signal S-parameter data measurd at 1.5 A total collector current and on continuous spectrum analyzer observation during high-power testing into various output load VSWR's at all phase angles. Table 2.13.1-5 is

Table 2.13.1-5 Output Dual Small-Signal S-Parameters At I_T = 1.5 A - 4:1 Coaxial Transformer With Balun Circuit

FREQ	S11		S21		S12		S22		S21	STAB	SGN
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	db	K	B1
1.00000	0.955	163	0.393	-171	0.002	-6	0.955	-118	-8.11	5.60	+
2.00000	0.724	145	1.820	139	0.007	-49	0.923	-157	5.20	2.91	+
3.00000	0.543	158	2.960	102	0.010	-96	0.871	-176	9.43	2.46	+
4.00000	0.631	149	3.820	102	0.012	-90	0.851	170	11.64	1.51	+
5.00000	0.462	143	6.370	79	0.019	-115	0.741	163	16.08	1.20	+
6.00000	0.412	155	7.530	56	0.021	-137	0.733	161	17.54	1.05	+
7.00000	0.467	161	8.170	40	0.020	-153	0.750	158	18.24	1.02	+
8.00000	0.484	162	8.740	28	0.019	-165	0.776	152	18.83	1.01	+
9.00000	0.513	160	9.310	17	0.019	-173	0.794	146	19.38	0.94	+
10.00000	0.537	157	9.920	7	0.018	180	0.813	139	19.93	0.91	+
11.00000	0.556	154	10.560	-2	0.018	175	0.822	132	20.47	0.86	+
12.00000	0.575	151	11.220	-12	0.017	171	0.832	125	21.00	0.85	+
13.00000	0.589	148	11.820	-21	0.016	167	0.832	117	21.45	0.86	+
14.00000	0.609	145	12.300	-31	0.015	165	0.832	109	21.80	0.87	+
15.00000	0.631	141	12.710	-41	0.015	164	0.813	100	22.08	0.87	+
16.00000	0.653	137	13.110	-50	0.015	165	0.794	92	22.35	0.85	+
17.00000	0.668	133	13.230	-60	0.015	165	0.767	83	22.43	0.86	+
18.00000	0.692	128	13.370	-69	0.015	165	0.733	75	22.52	0.85	+
19.00000	0.708	123	13.350	-78	0.016	165	0.692	66	22.51	0.82	+
20.00000	0.724	118	13.170	-87	0.017	165	0.653	58	22.39	0.79	+

FREQ	S11		S21		S12		S22		S21	STAB	SGN
MHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	db	K	B1
20.00000	0.724	119	13.300	-88	0.017	164	0.653	58	22.48	0.81	+
30.00000	0.781	62	10.480	-159	0.027	133	0.339	-14	20.41	0.68	+
40.00000	0.676	-1	8.370	146	0.033	93	0.260	-75	18.45	0.93	+
50.00000	0.624	-71	6.930	94	0.037	51	0.257	-116	16.81	1.10	+
60.00000	0.609	-138	5.840	44	0.039	9	0.260	-141	15.33	1.26	+
70.00000	0.582	159	5.280	-4	0.041	-33	0.269	-158	14.45	1.40	+
80.00000	0.436	89	5.250	-58	0.045	-81	0.282	-178	14.40	1.62	+
90.00000	0.331	-70	4.980	-127	0.045	-147	0.206	146	13.94	1.95	+
100.00000	0.758	-178	3.120	162	0.028	142	0.029	-144	9.88	2.48	+
110.00000	0.912	129	1.740	111	0.015	87	0.180	-117	4.81	3.30	+
120.00000	0.944	96	1.150	69	0.009	37	0.285	-130	1.21	5.04	+

a print-out of measured small-signal S-parameters as entered into SUPER-COMPACT for stability analysis. Critical frequencies are those where the stability factor, K, is less than one. Table 2.13.1-6 is the corresponding print-out of input and output stability circle locations. Because most of the critical frequency range is below the operating frequency range of the six-way power splitter and combiner, the amplifiers are isolated from external effects, having only to be stable with the impedances presented by the six-ways. Table 2.13.1-7 lists the minimum source and load reflection coefficients required for instability and the corresponding splitter and combiner reflection coefficients for each frequency, showing the large margin of

Table 2.13.1-6 Output Dual Stability Circles From Small-Signal S-Parameters

STABILITY CIRCLES

FREQ	*---- INPUT PLANE -----* LOCATION		RAD	STB	*---- OUTPUT PLANE ----* LOCATION		RAD	STB	GA MAX OR MSG	K	SGN B1
MHZ	MAG	ANG		REG	MAG	ANG		REG	dB		
1.00000	1.054	-163.3	0.010	OUT	1.054	117.7	0.010	OUT	12.5	5.60	+
2.00000	1.426	-151.3	0.172	OUT	1.089	155.8	0.032	OUT	16.6	2.91	+
3.00000	1.616	-161.9	0.309	OUT	1.124	175.4	0.053	OUT	18.0	2.46	+
4.00000	1.456	-158.0	0.334	OUT	1.144	-172.5	0.099	OUT	20.8	1.51	+
5.00000	1.839	-148.4	0.755	OUT	1.283	-164.6	0.244	OUT	22.5	1.20	+
6.00000	2.247	-141.2	1.218	OUT	1.331	-157.6	0.318	OUT	24.1	1.05	+
7.00000	2.582	-135.3	1.570	OUT	1.370	-151.2	0.364	OUT	25.2	1.02	+
8.00000	3.623	-127.9	2.618	OUT	1.387	-144.3	0.385	OUT	26.1	1.01	+
9.00000	5.865	-119.4	4.913	OUT	1.421	-137.1	0.439	OUT	26.9	0.94	+
10.00000	12.722	-111.5	11.808	OUT	1.431	-129.6	0.461	OUT	27.4	0.91	+
11.00000	49.687	76.3	50.547	IN	1.476	-121.5	0.524	OUT	27.7	0.86	+
12.00000	10.075	82.4	10.914	IN	1.501	-114.1	0.554	OUT	28.2	0.85	+
13.00000	9.181	84.7	10.030	IN	1.528	-105.7	0.579	OUT	28.7	0.86	+
14.00000	12.933	85.2	13.793	IN	1.550	-97.2	0.599	OUT	29.1	0.87	+
15.00000	28.875	-96.9	28.000	OUT	1.653	-86.2	0.707	OUT	29.3	0.87	+
16.00000	6.337	-98.3	5.467	OUT	1.750	-75.8	0.819	OUT	29.4	0.85	+
17.00000	3.671	-100.2	2.777	OUT	1.859	-64.8	0.929	OUT	29.5	0.86	+
18.00000	2.550	-101.1	1.646	OUT	2.032	-53.8	1.112	OUT	29.5	0.85	+
19.00000	2.138	-99.9	1.241	OUT	2.317	-40.8	1.427	OUT	29.2	0.82	+
20.00000	1.903	-97.9	1.013	OUT	2.675	-28.9	1.816	OUT	28.9	0.79	+

STABILITY CIRCLES

FREQ	*---- INPUT PLANE -----* LOCATION		RAD	STB	*---- OUTPUT PLANE ----* LOCATION		RAD	STB	GA MAX OR MSG	K	SGN B1
MHZ	MAG	ANG		REG	MAG	ANG		REG	dB		
20.00000	1.980	-98.5	1.083	OUT	2.905	-28.1	2.037	OUT	28.9	0.81	+
30.00000	1.444	-54.7	0.565	OUT	47.402	61.7	46.718	OUT	25.9	0.68	+
40.00000	1.632	5.3	0.660	OUT	10.438	100.8	9.501	OUT	24.0	0.93	+
50.00000	1.732	73.8	0.692	OUT	6.515	130.1	5.433	OUT	20.8	1.10	+
60.00000	1.736	140.6	0.637	OUT	5.399	153.8	4.192	OUT	18.7	1.26	+
70.00000	1.830	-155.5	0.675	OUT	5.291	173.6	3.979	OUT	17.3	1.40	+
80.00000	2.857	-82.4	1.510	OUT	6.639	-167.0	5.143	OUT	16.1	1.62	+
90.00000	4.275	68.7	2.643	OUT	14.539	-148.9	12.688	OUT	14.9	1.95	+
100.00000	1.337	178.2	0.154	OUT	8.818	47.3	11.583	IN	13.7	2.48	+
110.00000	1.103	-129.0	0.033	OUT	1.883	-42.4	6.956	IN	12.6	3.30	+
120.00000	1.062	-96.1	0.013	OUT	5.452	115.1	2.316	OUT	11.1	5.04	+

Table 2.13.1-7 Output Dual Stability As A System Component

REFLECTION COEFFICIENTS (50-OHM SYSTEM)

FREQUENCY (MHz)	SPLITTER SOURCE	MAXIMUM SOURCE ALLOWED	COMBINER LOAD	MAXIMUM LOAD ALLOWED
5	0.653	1.000	0.794	1.000
10	0.427	0.914	0.543	0.970
15	0.327	0.875	0.376	0.946
20	0.266	0.890	0.266	0.859
30	0.170	0.879	0.120	0.684
40	0.079	0.972	0.033	0.937
50	0.038	1.000	0.055	1.000
60	0.093	1.000	0.093	1.000
70	0.122	1.000	0.098	1.000
80	0.102	1.000	0.067	1.000
90	0.032	1.000	0.107	1.000
100	0.164	1.000	0.292	1.000
110	0.380	1.000	0.501	1.000
120	0.569	1.000	0.700	1.000

Note: Maximum Source Allowed and Maximum Load Allowed refer to the maximum reflection coefficient source or load that may be placed on the amplifier while maintaining stability.

stability. Also, by noting that the inband S21 listings (in dB) of Table 2.13.1-5 are from 2.5 to 3.9 dB higher than the high-power gain readings of Table 2.13.1-4, it is apparent that the small-signal stability predictions are more severe than actual application, because the bias levels are higher, and the amplifier is not driven into compression. In fact, the amplifier has been driven to 50 watts of forward output power into an infinite load VSWR at all phase angles across the band without incident, and no spurious products were generated.

The photographs in Figures 2.13.1-3 and 2.13.1-4 show the spectral output of a breadboard output dual powered by the breadboard switching power supply. As with the driver duals, performance was very close to that specified and will improve in the final layout with improved shielding and decoupling.

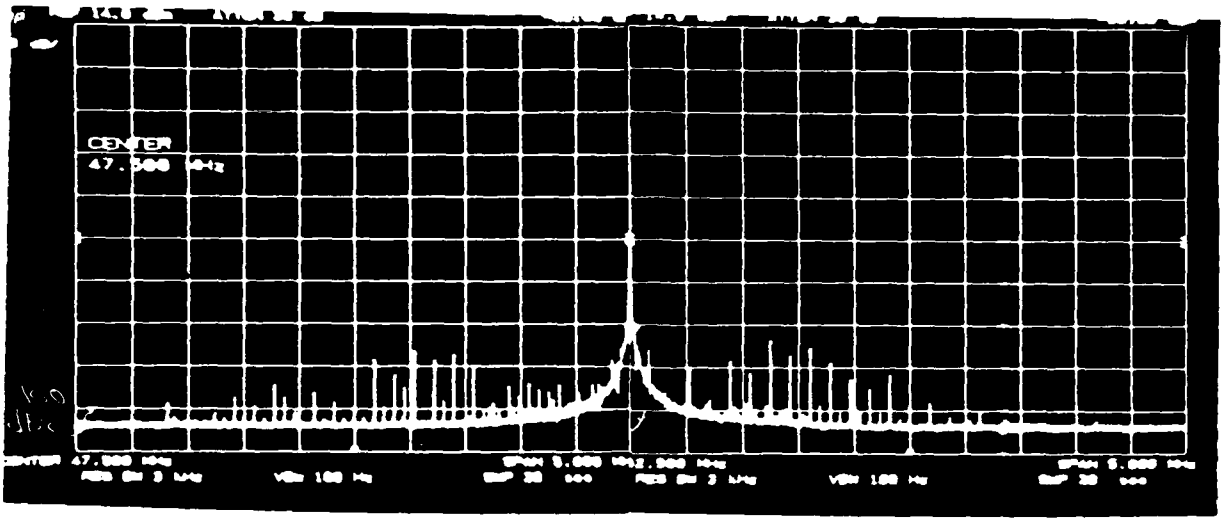


Figure 2.13.1-3 Spurious Outputs About 50 MHz Carrier (± 5 MHz)

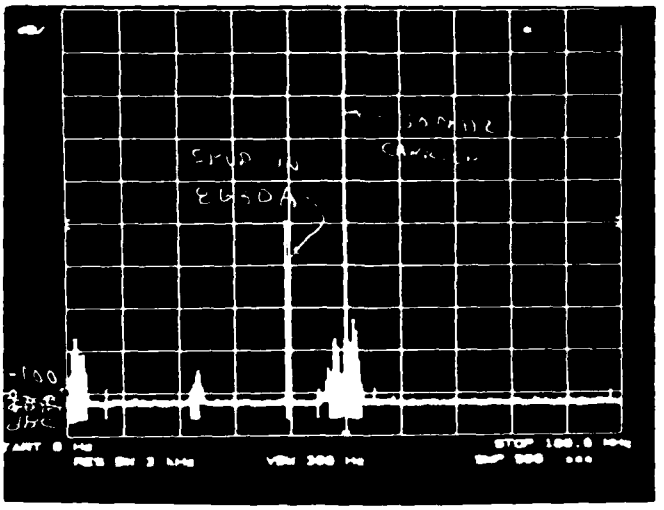


Figure 2.13.1-4 Spurious Outputs From DC To 100 MHz

A major concern of power amplifier designers dealing with mobile equipment is operation into less than ideal antenna load impedances. Every effort has been made to ensure a rugged, stable source of high-power RF into any load VSWR at any phase angle, with appropriate automatic power reduction as required. Figure 2.13.1-5 is a

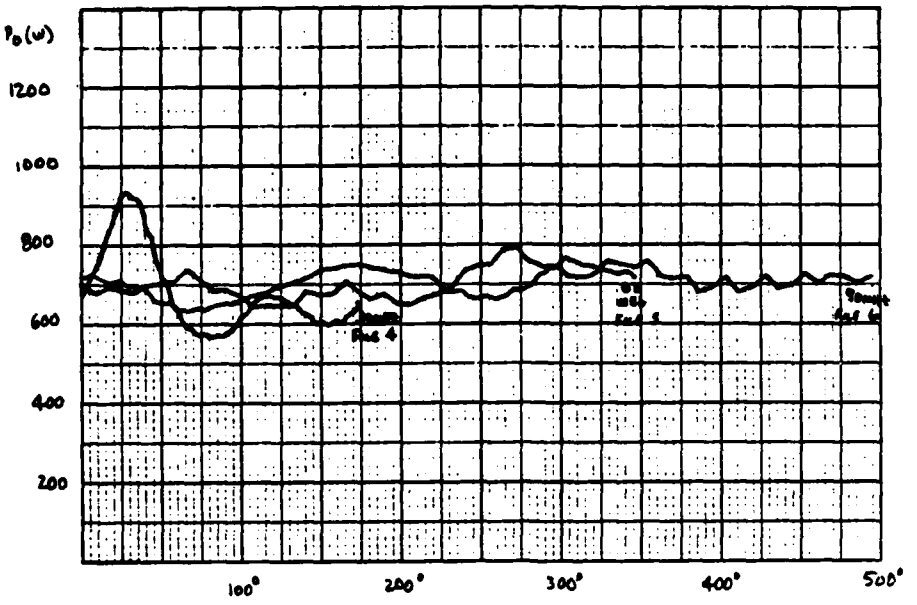


Figure 2.13.1-5 Predicted Total Output Power Into 3:1 Load VSWR

computer-generated graph of the predicted saturated output power of the six combined power amplifiers driving the six-way power combiner through phasing lines staggered six-inches per amplifier with an output load VSWR of 3:1 at all phase angles. The prediction is based on measured data of a single amplifier driven to an output limit of 200 watts, a current limit of 9 A, or a gain compression of 1.5 dB, assuming that one-half of any amplifier power imbalance will be absorbed in the combiner isolation resistors.

Gain balance between the six RF output amplifiers is accomplished by a select-at-test resistor adjustment on the base bias supply, a temperature compensated, low impedance, constant voltage source. Variable resistors were installed on the breadboard bias supply PC boards for convenience in performing laboratory tests. Figure 2.13.1-6 is a schematic of the bias supply, which is designed to operate on 3.6 to 4.4 VDC from an auxiliary set of windings on the 28-volt switching power supply. Figure 2.13.1-7 is a photograph of an output amplifier and bias supply mounted on the breadboard PA heatsink.

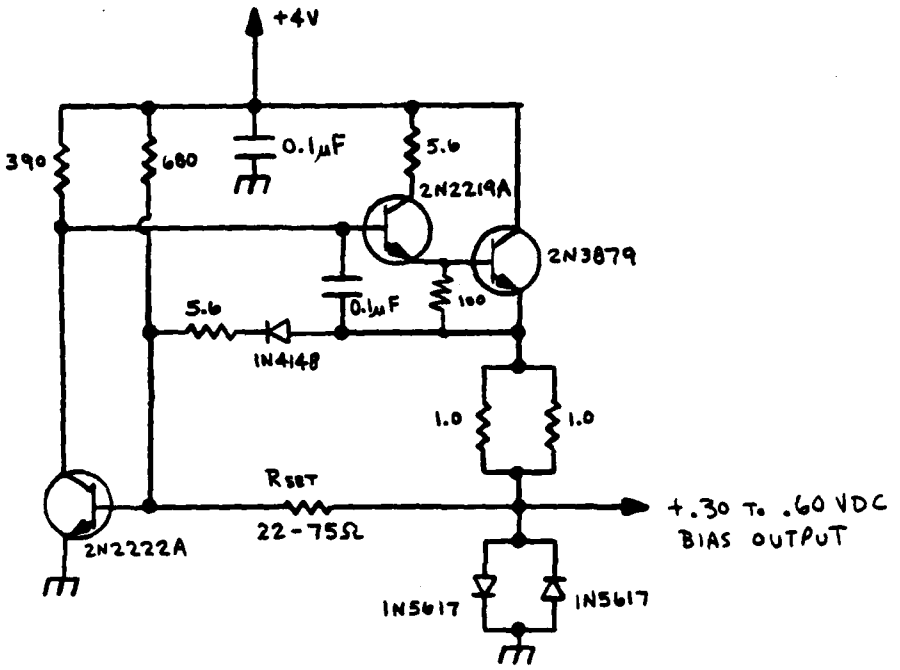


Figure 2.13.1-6 Temperature Compensated Bias Supply Schematic

Table 2.13.1-8 presents 100- and 125-watt output amplifier test data measured at +25, -51, and +65 degrees C. The amplifier quiescent collector current was constant at 1.0 milliamps over the entire temperature range, indicating the low bias levels and the accurate temperature tracking of the bias supply.

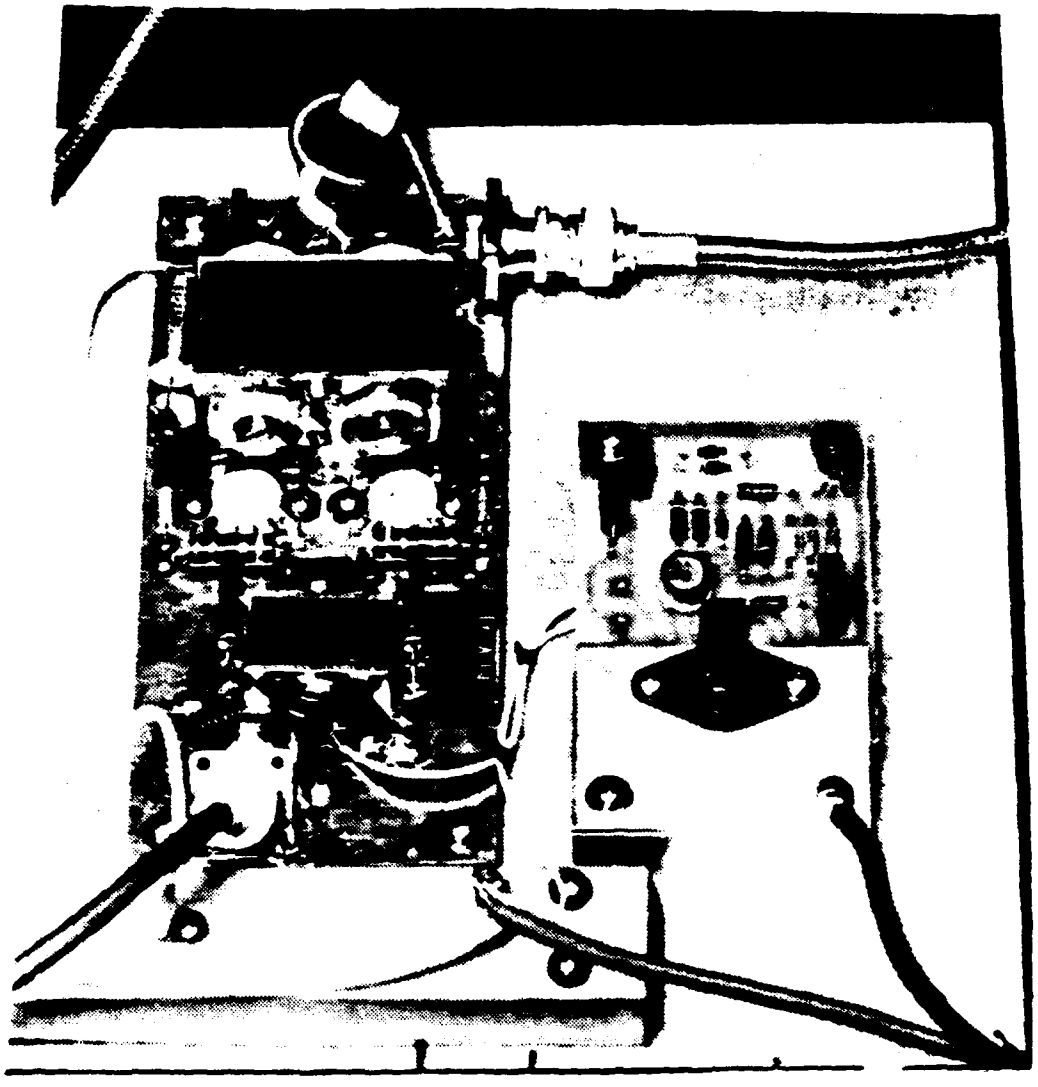


Figure 2.13.1-7 RF Output Amplifier And Bias Supply

Table 2.13.1-8 Output Amplifier Temperature Test Data

	FREQUENCY (MHz)						
	30	40	50	60	70	80	88
TEMPERATURE = 25°C							
Output Power = 100 Watts							
P_{IN} (W)	2.5	3.5	4.1	6.0	6.8	6.8	6.9
P_{REF} (W)	1.4	1.7	1.6	2.2	2.2	1.2	0.5
I_C (A)	6.6	6.4	6.2	6.2	6.3	6.4	7.0
Gain (dB)	16.0	14.6	13.9	12.2	11.7	11.7	11.6
Efficiency (%)	54.1	55.8	57.6	57.6	56.7	55.8	51.0
Return Loss (dB)	2.5	3.1	4.1	4.4	4.9	7.5	11.4
Output Power = 125 Watts							
P_{IN} (W)	3.4	5.4	5.8	8.4	9.1	8.2	8.6
P_{REF} (W)	2.0	2.6	2.4	3.0	2.8	1.7	0.6
I_C (A)	7.3	7.3	7.2	7.2	7.2	7.2	7.8
Gain (dB)	15.6	13.6	13.3	11.7	11.4	11.8	11.6
Efficiency (%)	61.1	61.1	62.0	62.0	62.0	62.0	57.2
Return Loss (dB)	2.3	3.2	3.8	4.5	5.1	6.8	11.6
TEMPERATURE = -51°C							
Output Power = 100 Watts							
P_{IN} (W)	2.6	3.2	4.4	6.4	7.2	7.8	7.4
P_{REF} (W)	1.5	1.6	1.8	2.3	2.2	1.6	0.8
I_C (A)	6.6	6.2	6.3	6.3	6.2	6.7	7.2
Gain (dB)	15.8	14.9	13.6	11.9	11.4	11.1	11.3
Efficiency (%)	54.1	57.6	56.7	56.7	57.6	53.3	49.6
Return Loss (dB)	2.4	3.0	3.9	4.4	5.1	6.9	9.7
Output Power = 125 Watts							
P_{IN} (W)	3.4	4.7	5.8	8.4	9.1	9.5	9.0
P_{REF} (W)	2.0	2.2	2.4	3.0	2.8	2.0	0.9
I_C (A)	7.4	7.2	7.2	7.1	7.1	7.4	8.0
Gain (dB)	15.6	14.3	13.3	11.7	11.4	11.2	11.4
Efficiency (%)	60.3	62.0	62.0	62.9	62.9	60.3	55.8
Return Loss (dB)	2.3	3.3	3.8	4.5	5.1	6.8	10.0

Table 2.13.1-8 Output Amplifier Temperature Test Data (Cont.)

	FREQUENCY (MHz)						
	30	40	50	60	70	80	88
TEMPERATURE = +65°C							
Output Power = 100 Watts							
P_{IN} (W)	2.5	3.2	4.2	6.4	6.2	5.7	7.1
P_{REF} (W)	1.4	1.5	1.6	2.3	2.1	1.3	0.6
I_C (A)	6.4	6.0	6.2	6.3	6.2	5.8	7.1
Gain (dB)	16.0	14.9	13.8	11.9	12.1	12.4	11.5
Efficiency (%)	55.8	59.5	57.6	56.7	57.6	61.6	50.3
Return Loss (dB)	2.5	3.3	4.2	4.4	4.7	6.4	10.7
Output Power = 125 Watts							
P_{IN} (W)	3.5	5.1	6.3	9.4	8.4	7.0	9.2
P_{REF} (W)	2.0	2.4	2.4	3.3	3.7	1.6	0.8
I_C (A)	7.2	7.0	7.2	7.4	7.0	6.5	8.0
Gain (dB)	15.5	13.9	12.9	11.2	11.7	12.5	11.3
Efficiency (%)	62.0	63.8	62.0	60.3	63.8	68.7	55.8
Return Loss (dB)	2.4	3.3	4.2	4.5	4.9	6.4	10.6

2.13.2 Output Amplifier Power Supply Design

The output amplifier power supply design is tightly integrated with the RF amplifier design in the output module. The power supply contains both its own BITE and control circuits as well as the BITE information and protection functions for the RF amplifier. Current sense circuits and foldback protection to limit the power available to the RF transistors are used to acheive these requirements for the design.

Technical information concerning the power supply design, development, and test efforts is contained within Section 2.6 of this report.

3.0 AMPLIFIER DESIGN STATUS

The amplifier module design status is well-represented by the design documentation and test data presented in Section 2 of this report. The key elements of the amplifier have been designed and breadboarded with the exception of the system controller. Integration testing of the entire RF chain is continuing, and no particular problems have occurred to date with the exception of test equipment RF pickup problems resulting from the lack of shielding of the open breadboard.

Examining the design status on a module-by-module basis:

A1 Chassis - The major layout efforts are complete and drawings for the casting have been finished. A purchase order has been placed for the casting with Armstrong Molding of Syracuse, New York, and two initial units, one for drop testing and one for dimensional check before approval of the final fabrication units are expected within 10 weeks. The design of the motherboard has not extended beyond basic concept definition, and the final layout of this unit will be the last design task performed.

A2 BITE/Monitor - A hardware design for the controller circuits has been completed based on the interfaces and functions defined. A hardware top-level functional flow-chart is in the final stages of development and, when completed, will be the basis for the controller software design. Some effort has been made to develop processor initialization and self-check routines, but the major software effort remains.

A3 Coax Relay/RF Bypass - The circuits of this module design are complete and an initial layout performed. To complete this module, only a final layout and PCB layout task remain.

A4 Power Input Assembly - The power control and input circuits have been designed and a layout performed of the mechanical mounting and interconnection.

A5 Control Circuit Power Supply - The control power supply design has been completed and tested. Some additional design verification data is being taken, and the final layout and PCB layout tasks have not been performed.

A6 Filter/Directional Coupler - The filter, coupler, and power control control circuit designs are basically complete and have been breadboarded and initial tests performed. Some changes are being made to the filter bandpass response for the final units to reduce loss at the upper end of the passband, and final testing of the loop reference and BITE circuits is now in progress. Some testing of the control circuits with the integrated amplifier also remains to be performed, as does the final PCB layout of the module.

A7 RF Input Processor - The design and testing of this module has been completed, with a initial PCB and module layout also performed.

A8 Six-Way Splitter - The splitter design, test, and layout efforts are complete, with the PCB designs now being transfered to final artwork and film for fabrication.

A9 Six-Way Combiner - The combiner status is the same as the splitter (A8).

A10 Driver Amplifier Power Supply - The power supply design is complete and has been tested, and only final packaging and transfer of the output amplifier power supply PCB layout to this design need to be performed.

A11 RF Driver Amplifier - The amplifier design is complete and the module has been packaged. A preliminary PCB layout is also complete and is ready for transfer to final artwork and film for fabrication.

A12 - A17 RF Output Amplifier - The RF amplifier and power supply designs are complete and packaging and PCB layout efforts also complete. These boards are now being transfered to final artwork and film. The module casting design and drawings are also complete, and a purchase order has been placed with Ceremet, Inc. of Allentown, Pennsylvania for these parts.

As seen in this summary, the primary emphasis in the development is rapidly changing to final packaging and layout. Long-lead material orders placed earlier in the project are slowly beginning to arrive for the deliverable units. Final purchase orders for miscellaneous parts not already available are now being placed.

A program status review meeting was held with CECOM personnel on January 25, 1983 at ECI. At this meeting, the current design status and breadboard hardware were reviewed. Following this meeting, CECOM agreed to tailored requirements for CE01 and CE04 of MIL STD 461A, Notice 4 in order to preclude redesign problems in system EMI filters and power supplies. Changes to the EMI control plan and other documentation have been made to reflect this requirements change.

Formal notification of changes to the contract to reflect the deletion of the manual keying circuits and the addition of the RF power control switch have finally been received. The outstanding GFE power connectors for the RT-246/VRC radios have also been received. Electrical acceptance tests on the GFE RT-246/VRC radios showed these units to be deficient in several areas, but the units are being used until a replacement decision is reached by CECOM.

4.0 FUTURE EFFORT

As stated in Section 3, the design effort is rapidly transfering to layout and final packaging. During the next reporting period, in addition to the packaging tasks, the final functional software design along with assignment of power levels during protect modes of operation will be performed. Remaining integration tasks for the breadboard such as the addition of the control loop and testing under load VSWRs will also be performed.

Fabrication of machine parts and PCBs for the deliverable hardware is also scheduled to begin within the next quarter. Orders will be placed for parts to complete the build effort. Documentation efforts including schematics and assembly drawings will continue. The amplifier Test Plan is also underway and scheduled for delivery.

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